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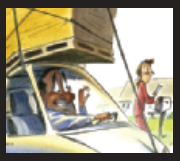

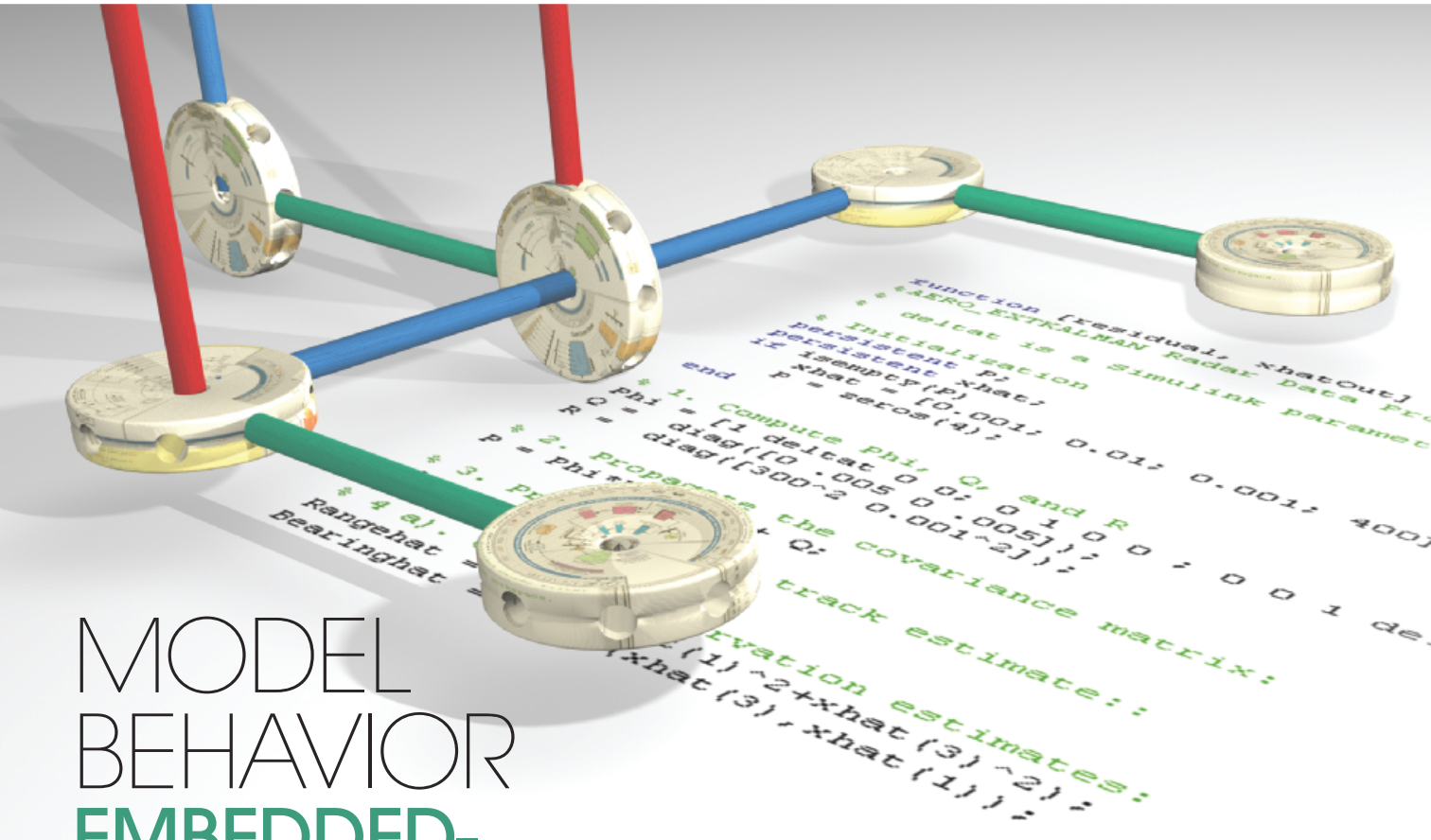

MODEL BEHAVIOR

EMBEDDED-SOFTWARE SHORT CUTS

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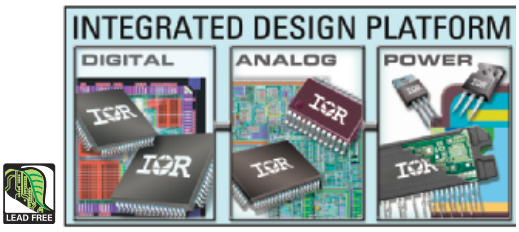

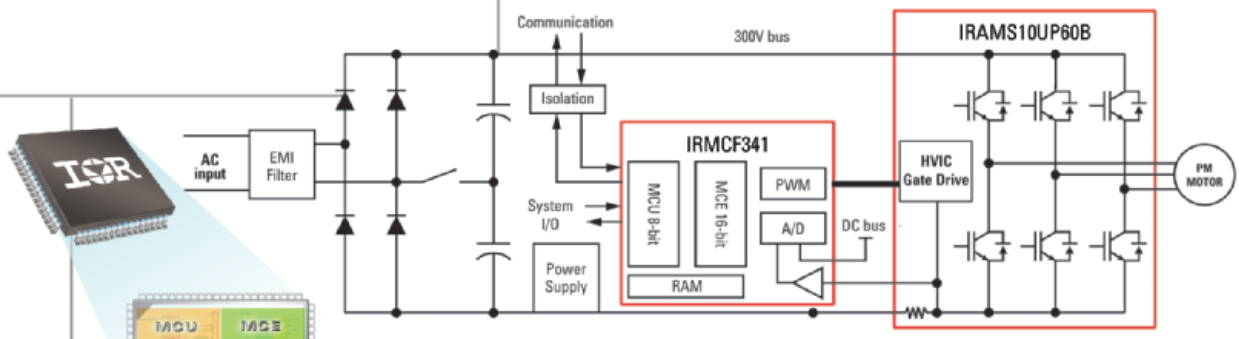

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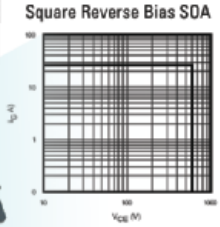

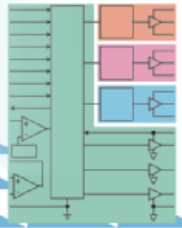

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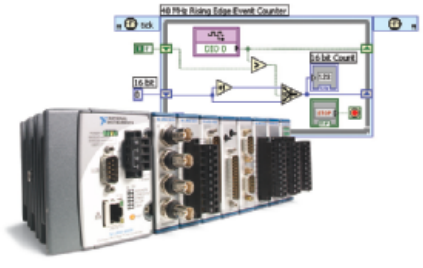

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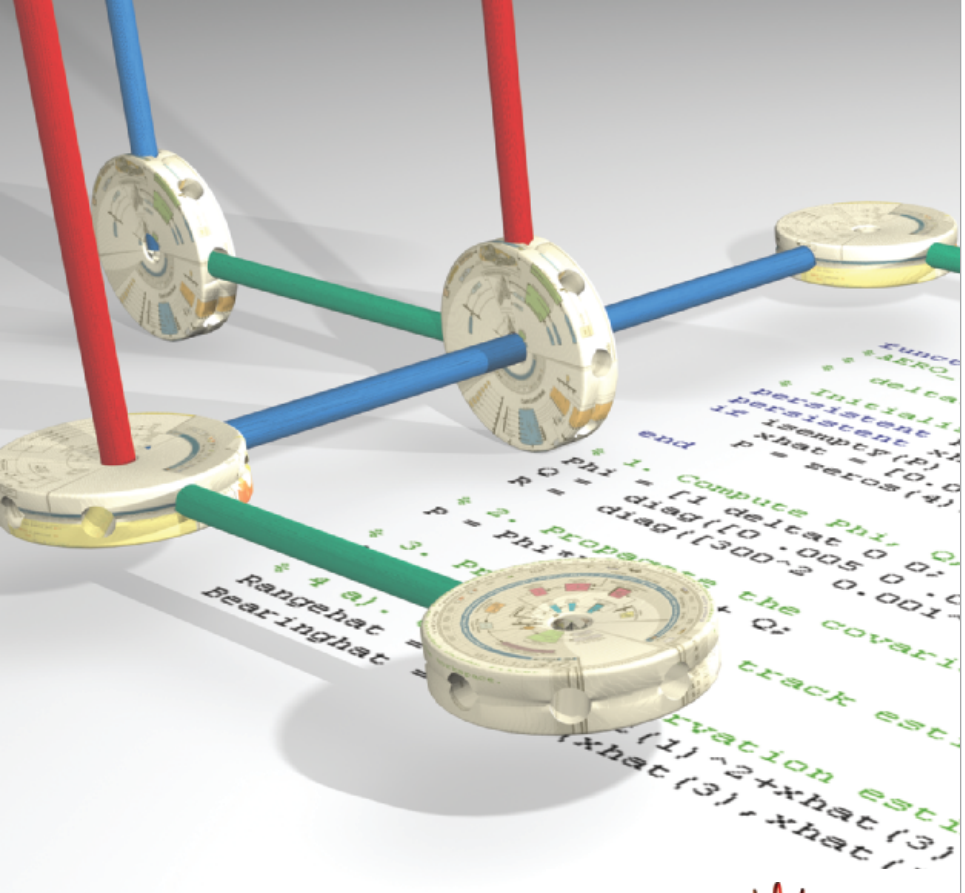


EDN contents

1.18.07

Agile software empowers wireless-sensor networks

 Applications for wireless networks can range from home automation to large-scale environmental monitoring. With the freedom these wireless approaches offer, you can network the tundra as easily as the office.

by PJ Tanzillo, National Instruments

A logical approach to NVM integration in SOC design

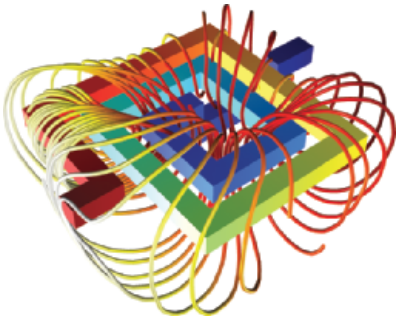
 SOC designers have several options for integrating NVM (nonvolatile memory) into their designs, so it's wise to weigh the availability and numerous trade-offs before jumping headfirst into integrating NVM into your SOC.

by Ann De Vries and Yanjun Ma, Impinj

Model behavior: creating embedded-software short cuts

 As embedded-system teams race to bring new products to market, designers are evaluating model-based development tools to deal with escalating software complexity.

by Warren Webb, Technical Editor



Beyond Spice

 Field-solver software can predict the behavior of circuits that operate at speeds and densities beyond the capabilities of Spice to properly model. Whether you are trying to verify signal integrity or designing an RFIC, you should know how field solvers could help your design.

by Paul Rako, Technical Editor

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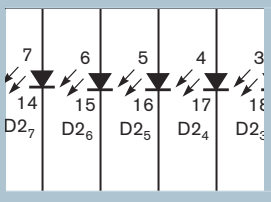

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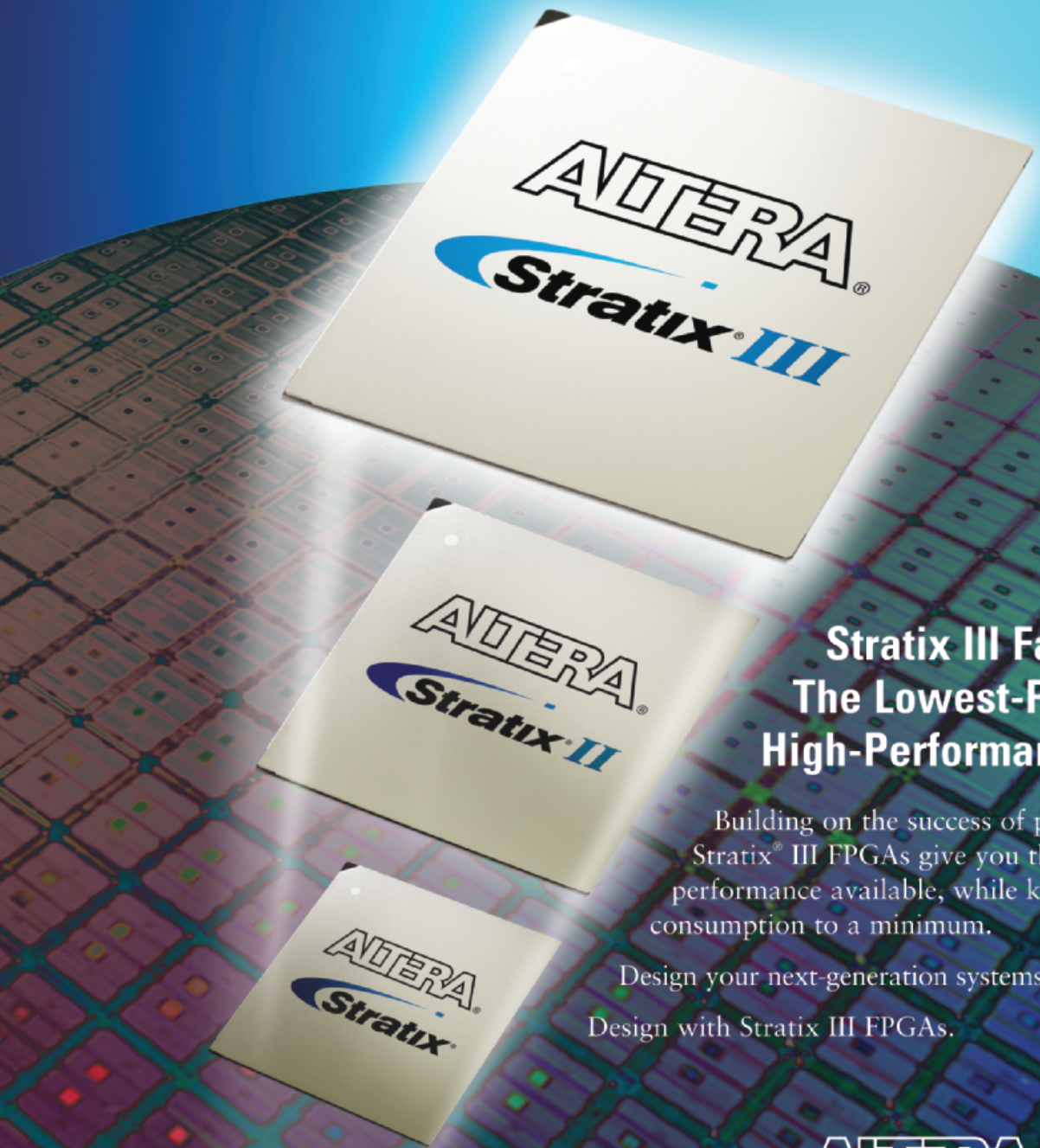

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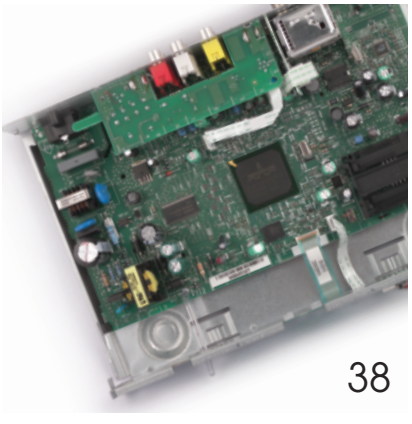

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DEPARTMENTS & COLUMNS

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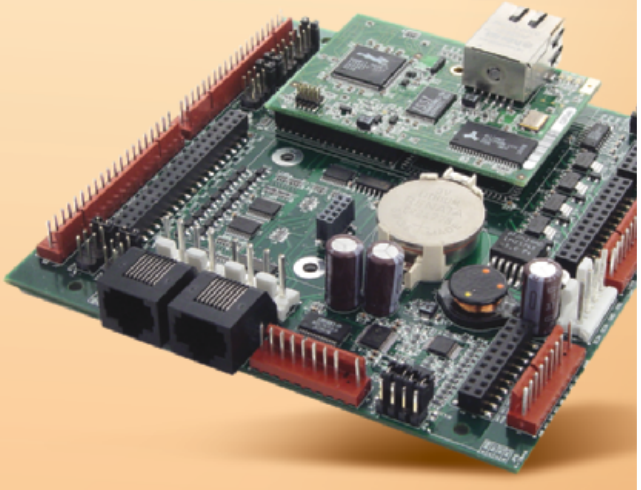

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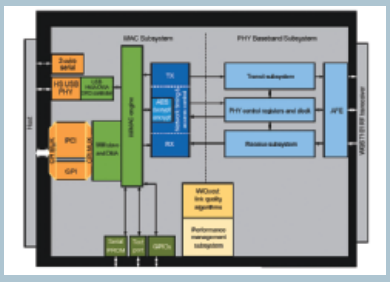

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WiQuest adds video support to Wireless USB
For months now, rarely a week has passed when one Wireless USB player or another hasn't touted a chip compatible with the specifications that the WiMedia Alliance has shepherded.
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Denali offers MLC and SLC NAND-controller core, development software
Denali Software Inc is expanding its implementation IP (intellectual-property) portfolio, introducing a new controller core for MLC (multilevel-cell) and SLC (single-level-cell) NAND devices.
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Blaze DFM's dummy-fill-synthesis tool has smarts
Blaze DFM is following up its mid-2006 release of its Blaze MO gate-CD biasing/leakage control tool with a dummy-fill "synthesis" tool.
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INTRODUCING: EMBEDDED PROCESSING

In this new blog, Technical Editor Robert Cravotta explores processor and software-processing architectures and the impact they have on system and software development.
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HOT 100 PRODUCTS of 2006
As 2007 gets underway and we prepare for a whole new batch of hot products in the year to come, take a look back at the ones to beat from 2006! Our list distills the most innovative and significant products of the year, including process technologies, power sources, storage devices, processors, intellectual-property cores, communication controllers, test instruments, embedded boards, EDA tools, and more.
→ www.edn.com/2006hot100

BY ROBERT GARDNER, EXECUTIVE DIRECTOR, EDAC

EDA Consortium: the Market Statistics Service

Editor's note: In two 2006 columns, *EDN* Senior Editor Mike Santarini took EDAC (Electronic Design Automation Consortium) to task for changes in how they report market numbers (www.edn.com/article/CA6387027 and www.edn.com/article/CA6298273. EDAC's Executive Director Robert Gardner responds here to those columns.

I'd like to shine some light on EDAC's MSS (Market Statistics Service) and talk about the value it provides. EDAC created the MSS more than 10 years ago to give industry members timely information about EDA revenue by market segment. The MSS releases the top-line industry-revenue numbers to the public each quarter, and paying subscribers receive breakdowns by more detailed product segments. The service is available for purchase from EDAC, with discounts for consortium members and companies that report their own data.

Although some have compared the MSS report with the Gartner/Dataquest report, it actually serves a different purpose. The Gartner/Dataquest report was perhaps the best-known and most detailed source of market numbers in EDA, providing market-share numbers and segment-growth forecasts. Gartner/Dataquest, however, published only annual numbers. The EDAC MSS report focuses on providing a quarterly snapshot of EDA revenue by product categories and region, offering a timely barometer of the industry.

The MSS has reported SIP (semiconductor-intellectual-property) data as a separate category since 1997, so it isn't a new addition. From 1997 to 2004, the MSS SIP category grew from having two subcategories to six subcategories. In addition, EDAC's quarterly press announcements publicly broke out SIP market-segment revenue. As IP (design reuse) became an increasing part of both EDA customers' speeding their designs to market and the product lines of many EDA companies, it made sense for EDAC to review the SIP-category reporting. In 2004, EDAC announced its work with the VSIA (Virtual Socket Initiative Alliance) to define approximately 40 additional SIP-product subcategories for the MSS. When making this decision, EDAC consulted with the VSIA to determine reasonable SIP-product subcategories. We also continued to reach out to IP companies to report their revenue numbers to EDAC. IP companies have since joined EDAC, and two of their leaders have joined our board: John Bourgoin, president and chief executive officer of MIPS Technology, and Sanjay Srivastava, president and chief executive officer of Denali Software. Another change that took place is that, in October 2005, EDAC announced its decision to include the publicly available numbers of nonreporting IP companies. EDAC includes all available market data to give the best picture of what's happening in the SIP-product segments. EDAC separately breaks out the nonreporting IP companies in the report so that a recipient of the report can exclude them from analysis if he or she wishes.

The inclusion of IP data does, of course, change the overall revenue that the MSS reports, but recipients of the report still get the full breakdown by product segment. The process is transparent, and any company that doesn't wish to include IP in its own internal analysis of the market can remove it.

To ensure the integrity of reporting, individual companies report their revenue—divided into the established product segments—to audit company PriceWaterhouseCoopers. The audit company then reports total revenue by product segment, as well as by region.

Like any other report about a dynamic market, this report's results are approximate. New companies or segment reporting can create year-over-year comparison issues in the data. EDAC handles these issues by providing complete listings of all companies included in each segment's numbers. Each user of the report has complete information, so they can judge how best to use the data.

The MSS is a great service that provides useful data at an affordable price. The quarterly release of revenue breakdown by major category (computer-aided engineering, pc boards and multichip modules, IC physical design and verification, and SIP) is only a small piece of the entire report. If you have interest in EDA-market data, EDAC encourages you to examine the full report. EDN

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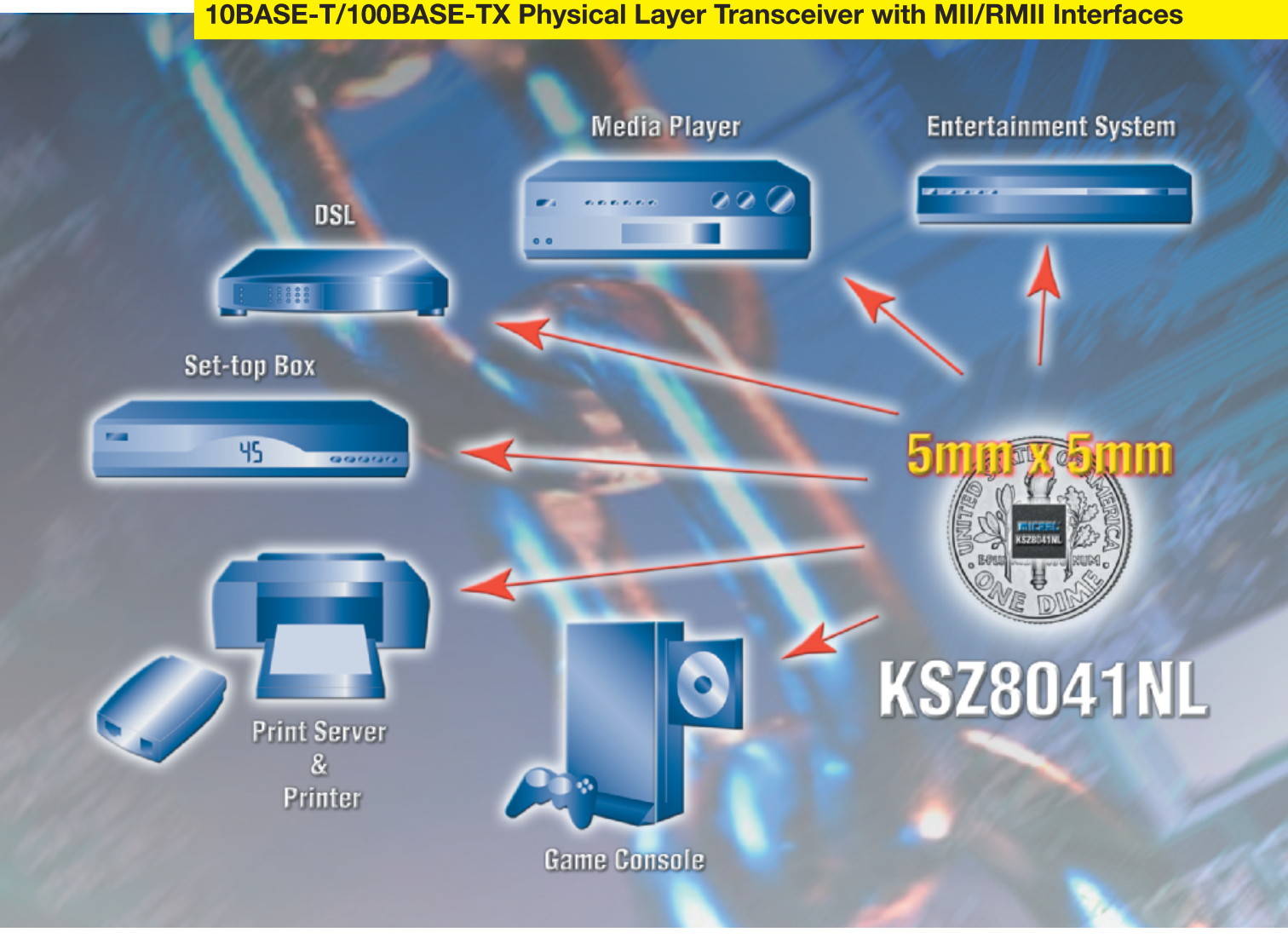

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PUBLISHER, *EDN* WORLDWIDE
John Schirmer
1-408-345-4402; fax: 1-408-345-4400;
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EDITOR IN CHIEF
Maury Wright, 1-858-748-6785;
mgwright@edn.com

EXECUTIVE EDITOR
Ron Wilson, 1-408-345-4427;
ronald.wilson@reedbusiness.com

MANAGING EDITOR
Kasey Clark
1-781-734-8436; fax: 1-781-290-3436;
kase@reedbusiness.com

EXECUTIVE EDITOR, ONLINE
Matthew Miller
1-781-734-8446; fax: 1-781-290-3446;
mdmiller@reedbusiness.com

SENIOR ART DIRECTOR
Mike O'Leary
1-781-734-8307; fax: 1-781-290-3307;
moleary@reedbusiness.com

EMBEDDED SYSTEMS
Warren Webb, Technical Editor
1-858-513-3713; fax: 1-858-486-3646;
wwebb@edn.com

ANALOG
Paul Rako, Technical Editor
1-408-745-1994;
paul.rako@reedbusiness.com

EDA, MEMORY, PROGRAMMABLE LOGIC
Michael Santarini, Senior Editor
1-408-345-4424;
michael.santarini@reedbusiness.com

MICROPROCESSORS, DSPs, TOOLS
Robert Cravotta, Technical Editor
1-661-296-5096; fax: 1-781-734-8070;
rcravotta@edn.com

MASS STORAGE, MULTIMEDIA, PCs AND PERIPHERALS
Brian Dipert, Senior Technical Editor
1-916-760-0159; fax: 1-781-734-8038;
bdipert@edn.com

POWER SOURCES, ONLINE INITIATIVES
Margery Conner, Technical Editor
1-805-461-8242; fax: 1-805-461-9640;
mconner@reedbusiness.com

DESIGN IDEAS EDITOR
Brad Thompson
edndesignideas@reedbusiness.com

SENIOR ASSOCIATE EDITOR
Frances T Granville, 1-781-734-8439;
fax: 1-781-290-3439;
f.granville@reedbusiness.com

ASSOCIATE EDITOR
Maura Hadro Butler, 1-908-347-9605;
mbutler@reedbusiness.com

EDITORIAL/WEB PRODUCTION MANAGER
Diane Malone, Manager
1-781-734-8445; fax: 1-781-290-3445
Steve Mahoney, Production/Editorial Coordinator
1-781-734-8442; fax: 1-781-290-3442
Melissa Annand, Newsletter/Editorial Coordinator
Contact for contributed technical articles
1-781-734-8443; fax: 1-781-290-3443
Adam Odoardi, Prepress Manager
1-781-734-8325; fax: 1-781-290-3325

CONTRIBUTING TECHNICAL EDITOR
Dan Strassberg, strassbergedn@att.net
Nicholas Cravotta, editor@nicholascravotta.com

COLUMNISTS
Howard Johnson, PhD;
Bonnie Baker; Joshua Israelsohn

PRODUCTION
Dorothy Buchholz, Group Production Director
1-781-734-8329
Kelly Jones, Production Manager
1-781-734-8328; fax: 1-781-734-8086
Linda Lepordo, Production Manager
1-781-734-8332; fax: 1-781-734-8086

EDN EUROPE
Graham Prophet, Editor, Reed Publishing
The Quadrant, Sutton, Surrey SM2 5AS
+44 118 935 1650; fax: +44 118 935 1670;
gprophet@reedbusiness.com

EDN ASIA
Raymond Wong, Managing Director/
Publishing Director
raymond.wong@rbi-asia.com
Kirtimaya Varma, Editor in Chief
kirti.varma@rbi-asia.com

EDN CHINA
William Zhang, Publisher and Editorial Director
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John Mu, Executive Editor
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EDN JAPAN
Katsuya Watanabe, Publisher
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t.mamoto@reedbusiness.jp

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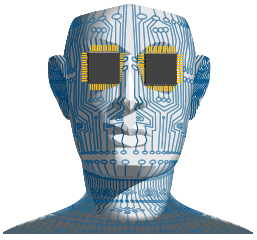

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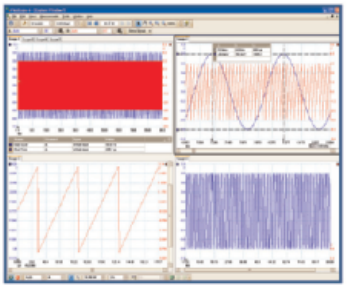

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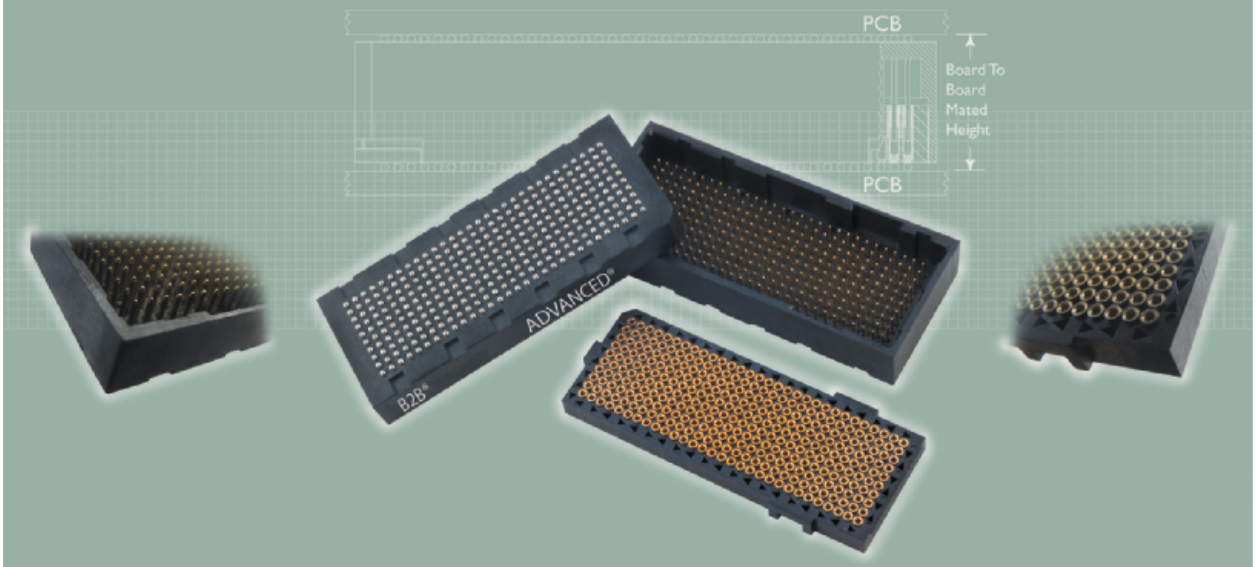

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Low-Voltage Current Loop Transmitter

— By Walt Bacharowski, Applications Manager

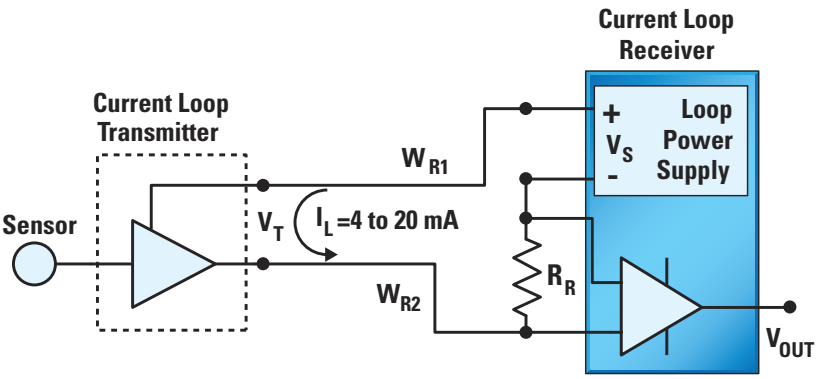

Figure 1. Current Loop Components and Connection

The 4 to 20 mA current loop, which is used extensively in industrial and process control systems, creates challenges for maximizing the operating loop length. In some cases, a very long loop is required and the combination of limited loop-power supply voltage and excessive loop wire resistance prevents it use. This article discusses the use of low-voltage amplifiers to minimize the transmitter's operating voltage requirements, which will maximize the operating loop length.

Typically, the current loop is powered from the receiver side while the transmitter controls the current flowing in the loop to indicate the value of the physical parameter being measured by the sensor. ***Figure 1*** shows the basic components and connection of a current loop.

The maximum distance between the transmitter and receiver is dependent on the power supply voltage (V_S), and the sum of the loop drops, which are the minimum transmitter voltage (V_T), the voltage drops across the wire resistance (W_{R1} and W_{R2}), and receiver resistor (R_R). In equation form:

EQ1 $$V_S = V_{WR1} + V_T + V_{WR2} + V_{RR}$$

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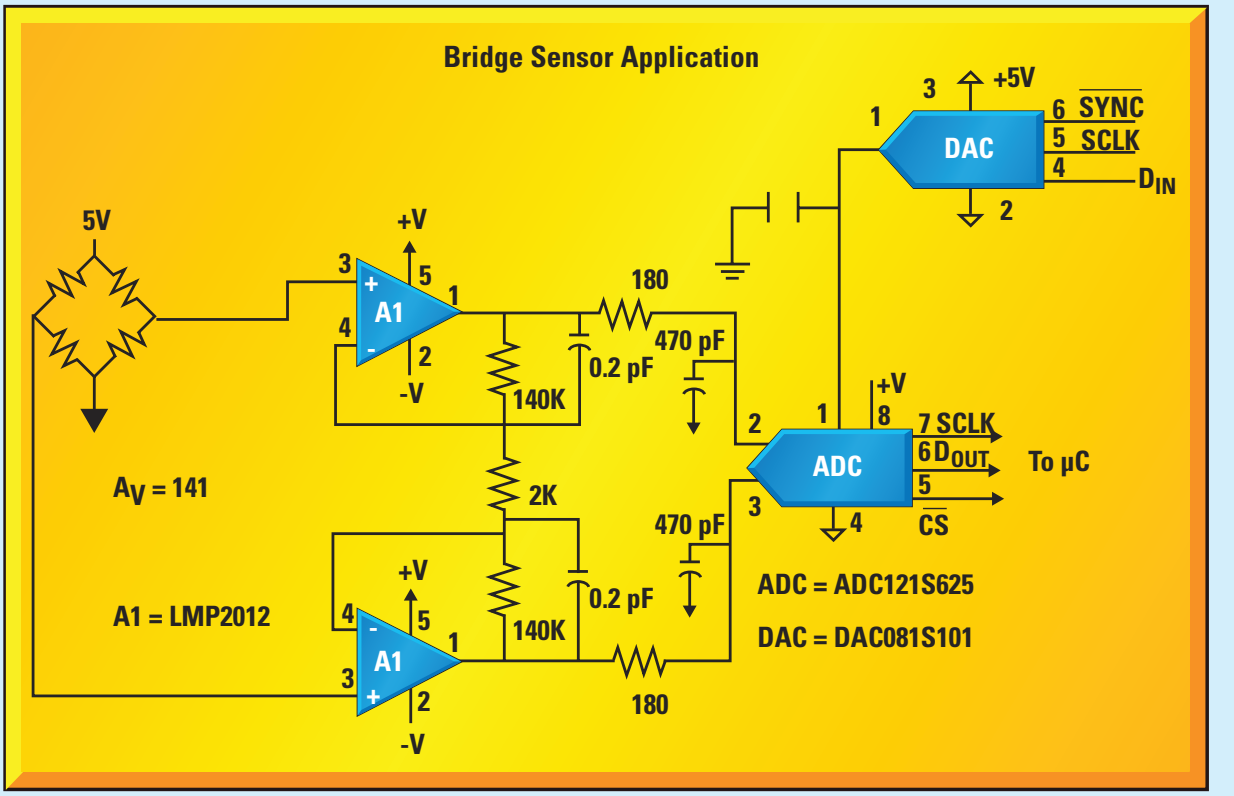

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Low-Voltage Current Loop Transmitter

Substituting the loop current and loop resistances into EQ1:

EQ2 $$V_S = I_L W_{R1} + V_T + I_L W_{R2} + I_L R_R$$

Given the wire's resistance in X Ohms per foot, the maximum loop current of 20 mA, the value of R_R equal to 10Ω, and the equal lengths of wire, EQ2 can be rearranged to calculate the maximum loop distance in terms the loop parameters:

EQ3 $$ft = \frac{V_S - V_T - 0.2}{0.04\ (X\ \Omega/ft)}$$

EQ3 illustrates three ways to increase the maximum loop length: (1) increase the loop power supply voltage, (2) increase the wire gage, which will reduce the wire's ohms per foot, or (3) reduce the minimum voltage required for the current loop transmitter operation, which is the focus of the following section.

The use of low voltage amplifiers, such as the LMV951, and low drop out voltage regulators, such as the LP2951, can reduce the minimum voltage required for the current loop transmitter. ***Figure 2*** shows the schematic of a loop-powered 4 to 20 mA transmitter, which will function with a minimum of 1.9V, and a 4 to 20 mA receiver.

In this example, a temperature sensor, such as the LM94022, provides a signal for the transmitter.

The components A1, Q1, and R1 through R5 form a voltage-to-current converter. The noninverting input of A1, pin 3, is the summing node for three signals, the loop current, offset current, and sensor signal voltage. The resistor R2 is the current shunt that measures the current flowing in the loop and is fed back through R3. The total loop current is the sum of the currents flowing in resistor R2 and R3, $I_L = I_{R2} + I_{R3}$. The amplifier, A1, forces the voltages at its inputs, pins 3 and 4, to be equal by forcing more or less current through R2. The result is that R2 and R3 have the same voltage across them. The ratio of the currents in R2 and R3 is the inverse of the resistor ratio:

EQ4 $$\left(\frac{I_{R2}}{I_{R3}} = \frac{R_3}{R_2}\right)$$

This highlights that the current in R3 is also part of the voltage-to-current conversion and is not an error current. An error source that will affect the loop current is the offset voltage of amplifier A1, which will add an error current to the loop current. At the minimum loop current of 4 mA, the voltage V2 is very close to 0.040V.

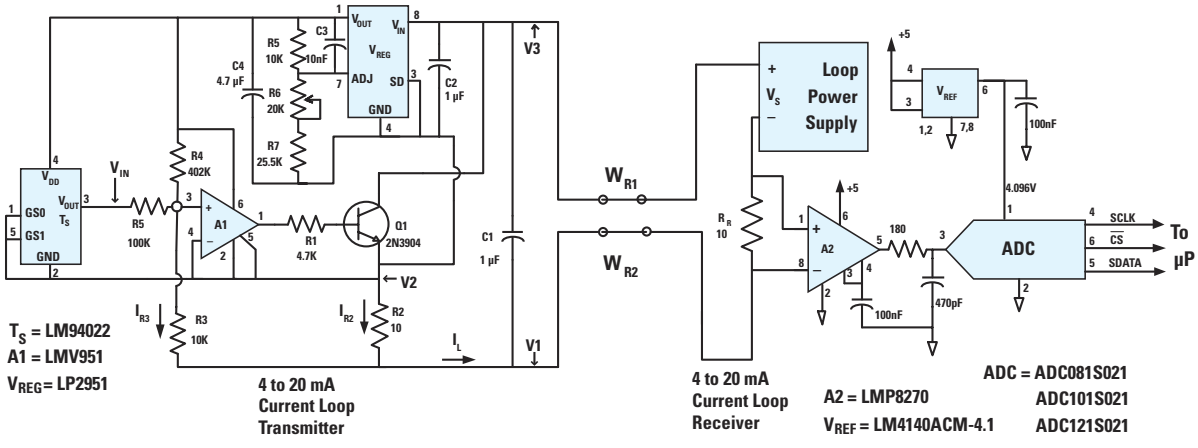

Figure 2. Loop-Powered Transmitter Schematic

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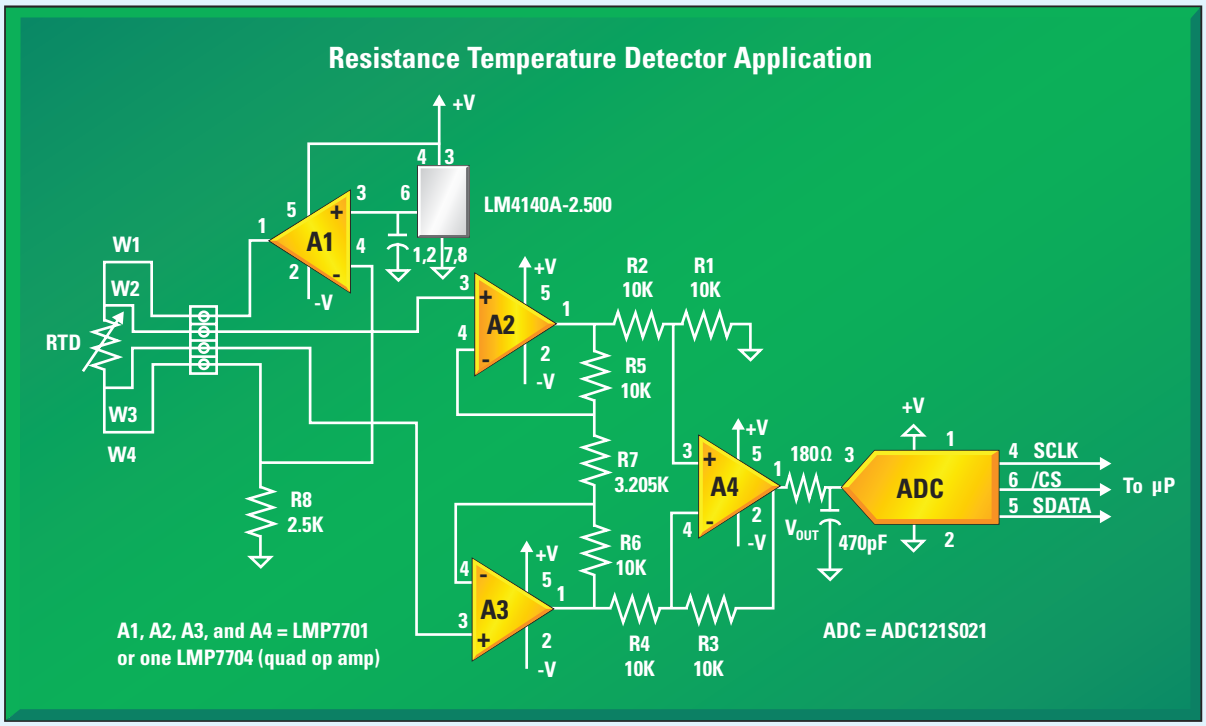

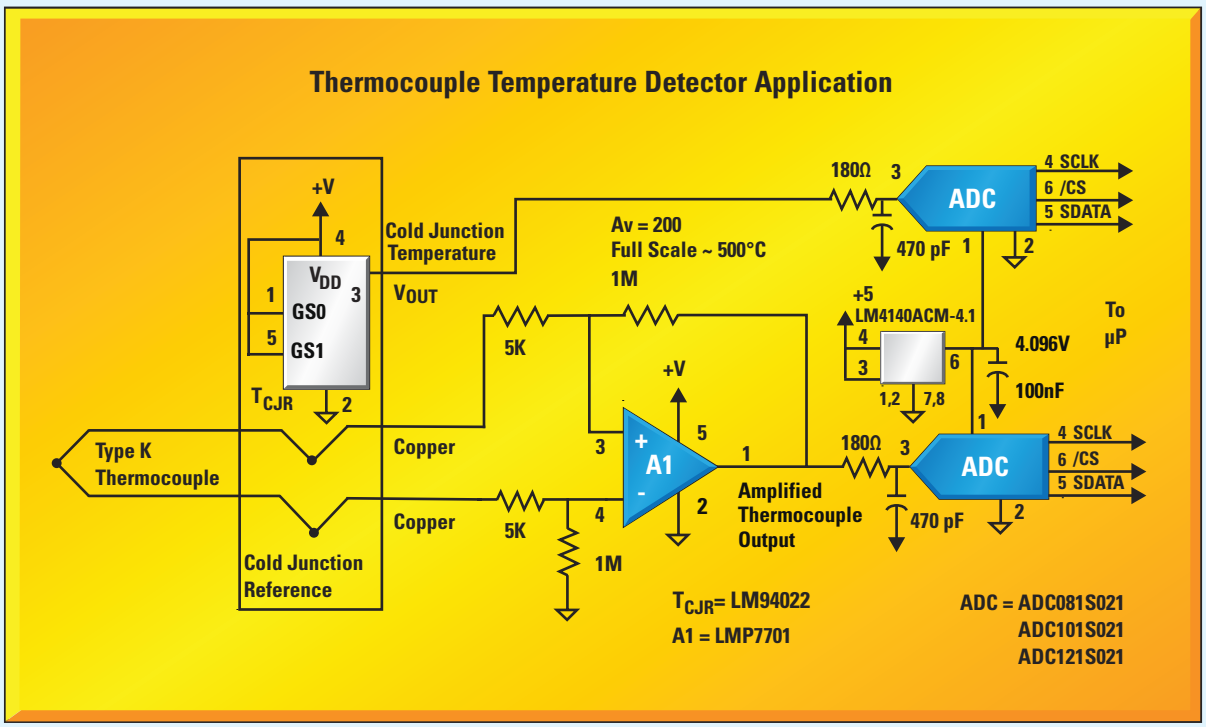

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LMP2011/12/14	25	0.015	2.7 to 5.25	120	130	130	3	35	-3
LMP7701/02/04	200	1	2.7 to 12	100	130	130	2.5	9	0.2
LMP7711/12	150	-1	1.8 to 5.5	100	100	110	17	5.8	0.1
LMP7715/16	150	-1	1.8 to 5.5	100	100	110	17	5.8	0.1

Precision Current Sense Amps

Product ID	Input Voltage Range	TCV_{OS} (µV/°C)	Fixed Gain (V/V)	Supply Voltage (V)	CMRR (dB)	Packaging
LMP8275	-2 to 16	30	20	4.75 to 5.5	80	SOIC-8
LMP8276	-2 to 16	30	20	4.75 to 5.5	80	SOIC-8
LMP8277	-2 to 16	30	14	4.75 to 5.5	80	SOIC-8

Low-Voltage Op Amps

Product ID	Typ Is/ Channel (µA)	Total Specified Supply Range (V)	Max V_{OS} (mV)	Max I_{BIAS} Over Temperature	Typ CMVR (V)	GBW (MHz)	Packaging
LMV651	110	2.7 to 5.5	1	80 nA (typ)	0 to 4.0	12	SC70-5, TSSOP-14
LMV791	1150/0.14	1.8 to 5.5	1.35	100 pA	-0.3 to 4.0	17	TSOT23-6, MSOP-10
LMV796	1150	1.8 to 5.5	1.35	100 pA	-0.3 to 4.0	17	SOT23-5, MSOP-8
LMV716	1600	2.7 to 5.0	5	130 pA	-0.3 to 2.2	5	MSOP-8
LPV531	425	2.7 to 5.5	4.5	10 pA	-0.3 to 3.8	4.6	TSOT23-6

ADCs for Single-Channel Applications

Product ID	Res	# of Inputs	Pin/Function Compatible	Throughput Rate (kSPS)	Input Type	Max Power 5V/3V (mW)	Supply (V)	Max INL (LBS)	Min SINAD (dB)	Packaging
ADC121S101	12	1		500 to 1000	Single ended	16/4.5	2.7 to 5.25	±1.1	70	SOT23-6, LLP-6
ADC121S051	12	1		200 to 500	Single ended	15.8/4.7	2.7 to 5.25	±1.0	70.3	SOT23-6, LLP-6
ADC121S021	12	1		50 to 200	Single ended	14.7/4.3	2.7 to 5.25	±1.0	70	SOT23-6, LLP-6
ADC101S101	10	1		500 to 1000	Single ended	16/4.5	2.7 to 5.25	±0.7	61	SOT23-6
ADC101S051	10	1		200 to 500	Single ended	13.7/4.3	2.7 to 5.25	±0.7	60.8	SOT23-6
ADC101S021	10	1		50 to 200	Single ended	12.6/4	2.7 to 5.25	±0.6	60.7	SOT23-6
ADC081S101	8	1		500 to 1000	Single ended	16/4.5	2.7 to 5.25	±0.3	49	SOT23-6
ADC081S051	8	1		200 to 500	Single ended	12.6/3.6	2.7 to 5.25	±0.3	49	SOT23-6
ADC081S021	8	1		50 to 200	Single ended	11.6/3.24	2.7 to 5.25	±0.3	49	SOT23-6
ADC121S625*	12	1		50 to 200	Differential	2.8	4.5 to 5.5	±1.0	68.5	MSOP-8
ADC121S705*	12	1		500 to 1000	Differential	16.5	4.5 to 5.5	±.95	69.5	MSOP-8

*Differential input, 200 to 500 kSPS thruput rate forthcoming

Low-Voltage Current Loop Transmitter

An offset voltage of 1 mV in A1 will cause an error of about 2.5% in I_{R3}:

EQ5 $$\frac{0.001V}{0.040V} \times 100 = 2.5\%$$

Because the ratio of I_{R2} to I_{R3} is 1000 to 1, an error of 2.5% in I_{R3} results in a 0.0025% error in the loop current.

The voltage supply requirements for the components in transmitter must be evaluated in order to determine the minimum operating voltage required by the transmitter. For this example, a full-scale sensor input signal of 1.6V is used and results in a 10 mA per volt scale factor:

EQ6 $$\frac{I_L MAX - I_L MIN}{V_{IN} MAX - V_{IN} MIN} = \frac{20\ mA - 4\ mA}{1.6V - 0V} = \frac{16\ mA}{1.6V} = 10\ mA/V$$

The minimum voltage required for the transmitter (V3 – V1) is the highest voltage requirement of the two paths from V3 to V1. Path one is from V3 to Q1 and R2 to V1. At the maximum loop current of 20 mA, the voltage drop across R2 is 0.2V (V2) and a collector emitter voltage of about 0.5V to stay out of saturation is a total of 0.7V. The second path is V2 plus the output voltage of the voltage regulator and its dropout voltage. The full-scale sensor input signal of 1.6V requires about a 1.65V output from the regulator and the dropout voltage of the voltage regulator is less then 50 mV. The path has a minimum voltage requirement of 1.9V (0.2 + 1.65 + 0.05). Note that the minimum operating voltage of the LMV951 is 0.9V so the minimum transmitter voltage could be reduced to about 1.3V by increasing the scale factor to 18 mA per volt. This is supported by the voltage regulator, V_R, which can be adjusted down to 1.25V, and with a drop out voltage of 50 mV, the loop transmitter can work down to 1.3V. The current loop transmitter functions by summing three signals: the loop current (R3), the offset current (R4), and the sensor (R5).

The loop current generates a voltage drop across resistor R2 such that V1 is negative with respect to V2 and then fed back through R3.

EQ7 $$V1 = V2 - R2(I_L)$$

The 4 to 20 mA current loop uses the offset current level of 4 mA to represent zero signal input. This is used as an open loop fault condition since zero current is a broken wire, transmitter failure, or another fault. The resistor R4 is connected to the output of the adjustable low drop-out voltage regulator to create the 4 mA offset current. Resistor R4, at 402 kΩ, sets approximately a 4 mA offset current when the output of the voltage regulator is 1.65V. The variable resistor R6 is used to set the loop current to 4 mA when the input signal is at zero volts. This adjustment compensates for error in the voltage regulator's output and resistor tolerance in R4, R5, and R7. The offset can be calibrated to 4 mA by measuring the voltage across R_R and adjusting R6 until the voltage across R_R is equal to 0.04V. The value of resistor R4 can be calculated for other supply voltages by equating the voltages at the amplifier's input pins and rearranging to solve for R4:

EQ8 $$R4 = \frac{R3 \times V_{OUT}}{R2 \times I_{R2}} - R_3$$

The resistor R5 is used to scale the signal input voltage to the 16 mA span of the loop current, and in this example, it is assumed the input signal span is 1.6V. The equation for calculating R5 can be developed by equating the voltages at the amplifier's input pins and rearranging to solve for R5. V_{IN} is the maximum signal input, 1.6V for this example, and I_{R2} is the change in output current, 16mA:

EQ9 $$R5 = \frac{R3 \times V_{IN}}{R2 \times I_{R2}}$$

This equation also indicates that changing the value of R5 can change the full-scale input voltage. A low resistance variable resistor could be used in

series with R5 to add a full-scale calibration as shown in the following schematic (*Figure 3*).

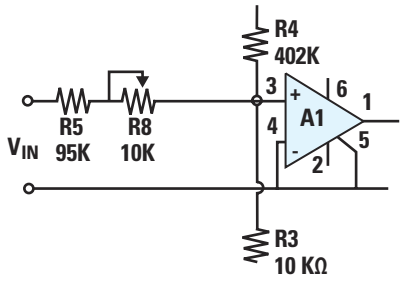

Figure 3. Input Calibration

In this example, a silicon temperature sensor is used as a signal source. The LM94022 is a low voltage, programmable gain temperature sensor that can be used to measure temperature from –50°C to 150°C. The schematic in *Figure 2* shows the LM94022's gain select pins connected to ground, or the lowest gain. With this gain, the sensor's output ranges from 1.299V for a temperature of –50° C to 0.183V for a temperature of 150°C.

As shown in *Figure 1*, the current loop transmitter accounts for only part of the voltage drop in the loop. The current loop receiver frequently uses a resistor, R_R in *Figure 1*, to generate a voltage drop that is used to measure the loop current. The measurement of the voltage across R_R can present some problems such as high common mode voltages, due to the loop power supply, as well as induced voltages from the environment. To overcome these measurement problems a differential amplifier, such as the LMP8270, can be used. The LMP8270 is a high common mode voltage differential amplifier with a fixed gain of 20. The gain of 20 also reduces the resistance of R_R, which reduces the loop voltage drop.

Referring to *Figure 2*, the voltage across resistor R_R is recovered from whatever common mode voltage exists on the current loop, up to 28V, and is amplified and drives the input to an Analog-to-Digital Converter (ADC). Internal to the LMP8270 is a differential amplifier with a gain of 10 followed by an amplifier with a gain of two. The internal connection between the two amplifiers is brought out to pins 3 and 4. Also internal to the LMP8270 is a 100 kΩ resistor in series with the output of the first amplifier. A low pass filter is easily implemented by connecting a capacitor from pins 3 and 4 to ground.

Figure 2 shows a 4.096V reference being used by the ADC, representing the full-scale input. The differential input voltage to the LMP8270 for a 4.096V output is 4.096/20 = 0.2048V. The value of R_R for a voltage drop of 0.2048V at a current of 20 mA is 0.2048/20 = 10.24Ω. A 10Ω resistor is used because it is a standard precision value. The result is an output voltage from A2 of 0.8V to 4.0V for a loop current of 4 mA to 20 mA.

The current loop transmitter was calibrated using the end points, 0V and 1.6V, as the input voltages while measuring the voltage across the R_R resistor. With 0.0V applied to the input the resistor R6 is adjusted until 40 mV is across R_R. With 1.6V on the input, resistor R8, see *Figure 3*, is adjusted until 200 mV is across R_R. *Figure 4* is the measured transfer function using a calibrated voltage source. The worst case deviation from a straight line was –8 µA, which is not observable on the graph in *Figure 4*.

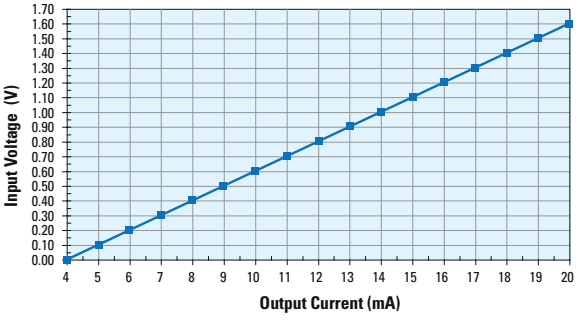

Figure 4. Output Current vs Input Voltage

In summary, by using a selection of components that function with very low supply voltages a current loop transmitter can be designed that operates with as little as 1.3V.

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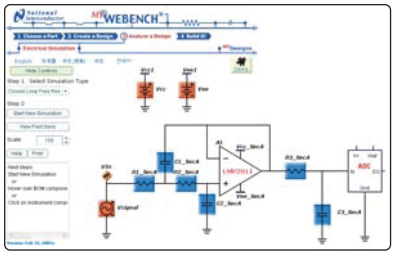

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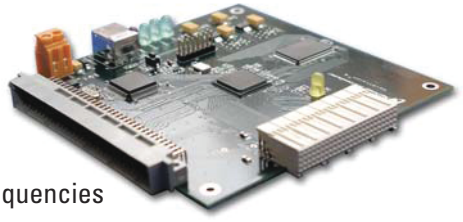

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LeCroy Corp's Windows-based QualiPHY, a hardware and software serial-data-compliance-test application, works with any of the company's 2-GHz or higher bandwidth real-time or sampling digital oscilloscopes and protocol analyzers. Targeting high-speed protocols, such as SATA (Serial Advanced Technology Attachment), FB-DIMM (fully buffered dual-inline-memory module), UWB (ultrawideband), Ethernet, USB, PCI Express, SAS (serial-attached small-computer-systems interface), and HDMI (high-definition-multimedia interface), the package provides digital- and analog-hardware engineers with an automated compliance-test tool for developing and validating devices' PHY (physical) layers in accordance with documents that the applicable standards organizations and special-interest groups have published.

QualiPHY features an intuitive graphical user interface that supports the industry's most popular serial-data standards and is common among them, eliminating the need for developers to learn new software for each project. Moreover, the expandable, modular architecture allows easy addition of support for more standards and suits the package to testing in such industry segments as computers and computer equipment, wireless and mobile multiservice (voice/data) products and systems, cable and IPTV (Internet Protocol-television) set-top boxes, and vending and gaming machines. The package's developers also had today's global-design environment in mind. A development team can conduct tests anywhere in the world through the supported scopes' IEEE 488 or LAN/WAN (local/wide-area-network) connections, which permit live access to signals from scopes in remote locations.

By incorporating an application framework that enables users to save every experimental result to an XML (Extensible Markup Language)-formatted record, the product goes beyond mere reporting and tabulating of test results. The software offers a choice of automatic HTML (Hypertext Markup Language), PDF (portable-document-format), or RTF (rich-text-format) report generation. The reports contain tabulated numerical values for each test. This approach benefits IC developers, who require comprehensive wafer and die characterization to define parametric performance and establish device-performance capability; system-level-validation teams that work in parallel development cycles and must combine, study, and interpret performance data and correlate test results with earlier runs; and manufacturing and production tests, which use control charts and other performance indicators to monitor key parameters.

QualiPHY prices range from $2995 each for versions that support USB and Ethernet to $6995 for a version that supports UWB. All versions accommodate modules that add support for more standards. **—by Dan Strassberg**

▷**LeCroy Corp**, www.lecroy.com.

FEEDBACK LOOP

"I was thinking the other day about how long it will be before we embed Bluetooth cell-phone transceivers in our ears. Not much different from some of the ear piercings I see these days. I was thinking about how difficult it would be to replace batteries, but now I think scratching your ear once in a while may do the trick!"

—Chris Woolpert, in *EDN*'s Feedback Loop at www.edn.com/article/CA6399099. Add your comments.

Low-cost, high-I/O-count FPGAs target display market

In an attempt to nab sockets in the market for low-cost, high-volume video displays, Xilinx has released an I/O-heavy version of its 90-nm Spartan-3 FPGAs. Before this release, Xilinx introduced a high-gate- and high-pin-count version of the device, the Spartan-3. The company then followed it up with a logic-heavy version, Spartan-3E. Now, the company is introducing its high-I/O-count Spartan-3A devices, targeting I/O-intensive applications, most notably, the emerging video-display market in mainland China.

Mark Moran, senior strategic-marketing manager for the general-products division at Xilinx, says that the new 3A devices excel as bridging functions, in differential signaling, and as memory interfaces. Moran notes that, in many of today's applications, companies create one giant ASIC device for several product derivatives and then add functions and support to FPGAs in combination with the ASICs for new or emerging interfaces. Doing so allows users to keep the same footprint on a pc board but create derivatives or initiate field upgrades as needed.

To serve the bridging function, the 3A supports the most popular I/O standards, including PCI (Peripheral Component Interconnect), PCIe (PCI Express), USB, CAN (controller-area network), SPI, and I^2C. To aid in differential signaling in displays, Xilinx has ensured that the device complies with both TMDS (transition-minimized differential signaling) and PPDS (point-to-point differential signaling). To help the larger chips adapt to the ever-growing and -changing memory world, Xilinx has added interfaces for DDR and DDR2.

Spartan-3A devices include two hibernate modes: one for 40% static-power reduction and one for 99% static-power reduction. Both modes have a wake-up time of less than 100 msec. The Spartan-3A also includes "device DNA" to help companies protect the designs they implement on FPGAs from piracy or cloning. "Device DNA is a unique serial number within each FPGA," says Moran. "We program it in at manufacturing time. Then, we allow the users to determine what authentication mechanism they want to use." Users can choose from several types of encryption mechanisms. They can change the authentication encryption at any time and even in the field. "You can change it from design model to design model, so, if you are concerned about cloning, you can change it however and whenever you want to," Moran says. "Because it is incorporated in the design, you can fix it, so when the design does not authenticate, you can stop the system from functioning by telling the system to turn off one or several global controls in the FPGA. If there is one thing FPGAs are not short on, it is global control."

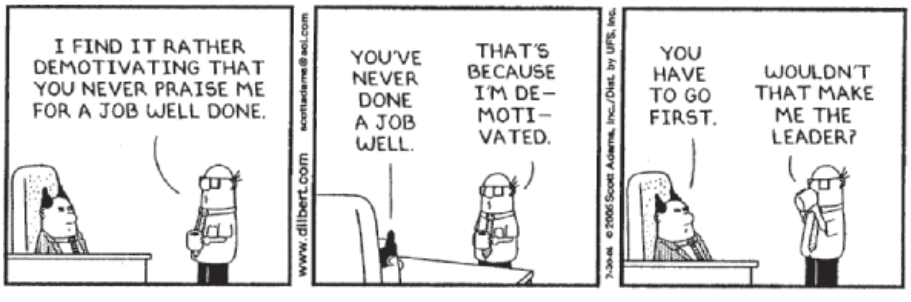
You can also configure the authentication circuitry. "You can, for example, allow a contract manufacturer to access the full chip for test purposes for, say, eight minutes—enough time to test the chip in the context of the system but not enough time to copy the design," says Moran. "Now, you have the ability to stop cloning, reverse-engineering, and overbuilding."

Xilinx expects full production of the 700,000-system-gate XC3S700A and the 1.4 million-system-gate XC3S1400A to begin in the first quarter of this year. The company plans to have the rest of its Spartan-3As in production by the second quarter of this year. The company also plans to offer 50,000-, 200,000-, and 400,000-gate versions. Prices for the XC3S700A and XC3S1400A devices are $11.95 and $16.95 (250,000), respectively. Starter kits are available now for $199.

—by Michael Santarini

▷**Xilinx**, www.xilinx.com.

DILBERT By Scott Adams



DATA-ACQUISITION MODULE FEATURES USB INTERFACE

01.18.07

Targeting test, security, and industrial-control applications, Sealevel Systems recently announced the first in a family of USB-compatible data-acquisition and -control modules. The SeaDAC MIO-26 includes 16 single-ended or eight differential, 12-bit analog inputs; two 12-bit DAC outputs; eight optically isolated digital inputs; and eight open-collector digital outputs. You can independently software-select each ADC input-voltage range and configure the device for measuring a 0- to 20-mA current loop.

The ADC channels feature 5-MHz bandwidth track/hold and 100k-sample/sec throughput. The module's DAC channels are independently jumper-selectable for a 0 to 5 or a 0 to 10V output range. The digital inputs are 5 to 30V dc, and the open-collector outputs are suitable for switching the 24V devices you commonly find in industrial-control applications.

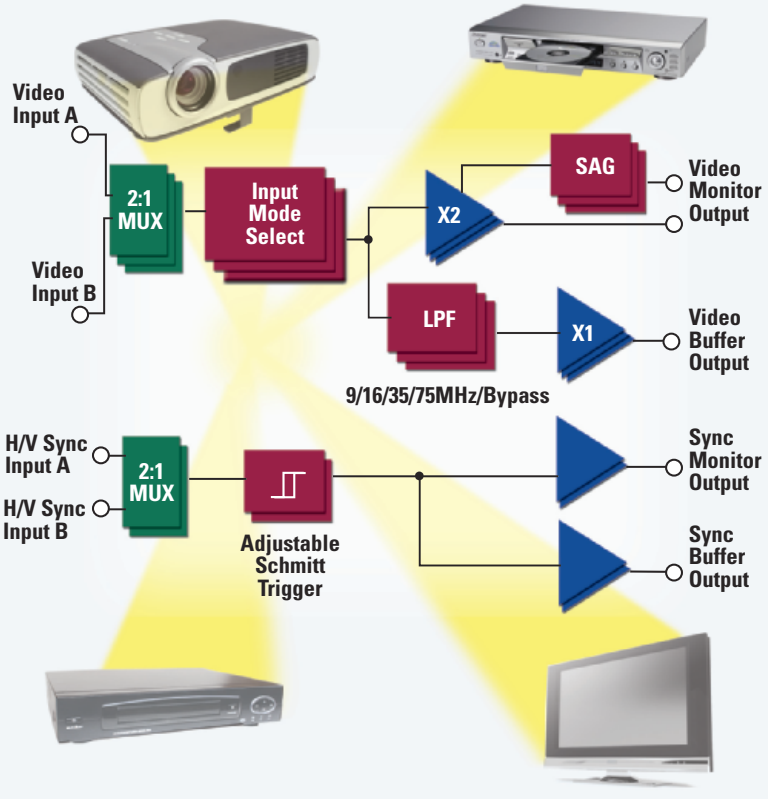
The SeaDAC MIO-26's standard operating-temperature range is 0 to 70°C, and an extended-temperature range of −40 to +85°C is optional. Application software can use the vendor's SeaMax library or industry-standard Modbus protocol. The module comes with diagnostic utilities and sample programs. Prices for the SeaDAC MIO-26 start at $479 (small volumes), and it is now available.

—by Warren Webb

▶**Sealevel Systems Inc, www.sealevel.com.**

First Triple Video Amp

Integrates HV Sync, Filters and I²C Control



Applications

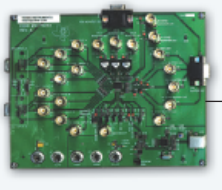
- Projectors
- Digital TVs
- Professional video systems
- Set-top boxes
- DLP® projectors/televisions

Features

- 3 video amplifiers for CVBS, S-video, EDTV, HDTV and RGB
- HV sync paths with adjustable Schmitt Trigger
- 2:1 input MUX
- I²C control of all functions/all channels
- Integrated low-pass filters on ADC buffer path
- Selectable input bias modes
- Monitor pass-through function
  - Passes input signal without filtering
  - 500MHz bandwidth and 1300V/µs slew rate
  - 6dB gain with SAG correction
- Pricing: $3.35 in 1k units

The **THS7327** from Texas Instruments integrates three analog video channels and two digital channels for HV sync, greatly simplifying system design and reducing component count. The three analog channels incorporate unity gain buffering and monitor feed-through paths to handle all standard video formats, including RGB, YPbPr and CVBS. Designers gain flexibility with the amplifier's I²C-programmable functions including: integrated 2:1 input multiplexers which enable switching of multiple video sources; fifth-order antialiasing filters to enable use with multiple video standards; and input bias modes.

For Samples, Evaluation Modules and Technical Information



www.ti.com/THS7327 ○ 800.477.8924, ext. 13477

Technology for Innovators™

Texas Instruments

IEEE 802.11n wireless-LAN market remains in conflict as draft-n battle looms

Does the IEEE 802.11n wireless-LAN spec even matter? Yes, we could use faster wireless-LAN technology and better range. The speed mainly matters for video delivery, although a higher maximum bandwidth also means that an access point can support more users. In reality, however, the Wi-Fi community has settled into a comfort zone in which 802.11g will be the de facto technology standard for a long time. Backward compatibility with that standard may be more important than "draft compatibility" with the next standard. Nonetheless, chip vendors, including relatively unknown Ralink (www.ralinktech.com), have been relentlessly pushing new draft-n chips, and new end products will almost surely have arrived at the CES (Consumer Electronics Show, www.cesweb.org), which took place in mid-January in Las Vegas.

Ralink claims that its new RT2800 chip set will offer the industry's longest range yet. To date, the company has had success primarily in value-priced products as opposed to at the premium end of the price range in which vendors push range and speed advantages. The company can't explicitly describe the design elements that enable the range, so we'll again wait for end products to see how they fare. The company does appear to have a size advantage in that its chip set, with all the necessary antennas for both frequency bands that 802.11n products require, can fit into a typical USB-style Wi-Fi package.

In other recent activity, Metalink (www.metalinkbb.com) revealed the second generation of its WLANPlus family, which also claims draft-n compatibility. Metalink targets consumer-electronics applications with claims that the product can carry HDTV streams. Marvell (www.marvell.com), meanwhile, announced that Gateway (www.gateway.com) would begin shipping PCs based on the draft-n Marvell TopDog chip.

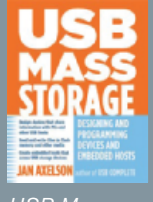
But does draft-n status carry any credibility? With the 802.11n standard development stretching years beyond what it should have, the Wi-Fi Alliance (www.wi-fi.org) has announced plans for draft-n compliance testing, but that testing won't start until the second quarter of 2007, when, with any luck, the 2.0 draft of the 802.11n standard will achieve more success at the ballot box. And one company, Airgo Networks (www.airgonetworks.com), has just announced its fourth-generation MIMO (multiple-input multiple-output) chip with the claim of draft 2.0 compatibility, despite the work that the standards body still needs to do.

The bigger news from Airgo, however, is that Qualcomm (www.qualcomm.com) recently acquired the MIMO pioneer. As noted on a recent *EDN* blog post, Qualcomm has in the past aggressively protected and profited from its IP (intellectual-property) portfolio, including CDMA (code-division-multiple-access) technology for mobile phones. Airgo's MIMO IP could receive the same attention (www.edn.com/blog/150000015/post/1860005786.html). At least one other Wi-FI pundit, *Wi-Fi Net News* (http://wifinetnews.com/archives/007182.html), had the same thought.

—by Maury Wright

PRACTICAL BOOK HELPS DEVELOPERS APPLY USB-INTERFACED MASS-STORAGE DEVICES

In technical writing, clarity is the name of the game. As someone who writes technical prose, I greatly admire Jan Axelson; she knows better than almost anybody else how to write clearly and how to explain complex technical issues so that her audience can understand them with minimal frustration. She has written many books on embedded-system topics, including *USB Complete Third Edition* (ISBN13 978-1-931448-02-4). Like her earlier books, her latest, *USB Mass Storage: Designing and Programming Devices and Embedded Hosts* (ISBN: 1-931448-04-3), aims at a person with a full plate of development work and looming deadlines who needs examples of practical ways to solve real and common problems.



USB Mass Storage is a practical guide to applying storage devices that interface using the ubiquitous bus.

The $29.95, 287-pg paperback is a guide to designing and programming devices that implement storage functions, including devices that transfer data through the USB interface. Storage devices include drives of all types, as well as many cameras, data loggers, and other devices that perform dedicated functions. Using flash memory and other current technologies, even the smallest devices can store lots of data. The book shows how to choose storage media, how to interface the media to a microcontroller or another CPU, and how to write device firmware to access the media and use USB to transfer data to and from storage. A comparison of media types helps in selecting media for a project. The media that Axelson considers include hard drives and flash-memory cards, such as the MMC (MultiMediaCard), SD (Secure Digital) Card, and CF (CompactFlash) cards. You will also learn what's involved in developing an embedded host that accesses off-the-shelf USB drives.

Covered protocols include the bulk-only transport protocol for the USB mass-storage class, SCSI (small-computer-system-interface) commands that USB mass-storage devices support, the MMC commands and SPI (serial-peripheral-interface) protocol that MMCs and SD Cards support, and FAT (file-allocation-table) systems for accessing files and directories. Code examples show how to implement the protocols. To complement the book, Axelson maintains a Web page (www.lvr.com/mass_storage.htm) with links to articles, program code, and other areas of interest to USB mass-storage developers. **—by Dan Strassberg**

▶Lakeview Research LLC, www.lvr.com.

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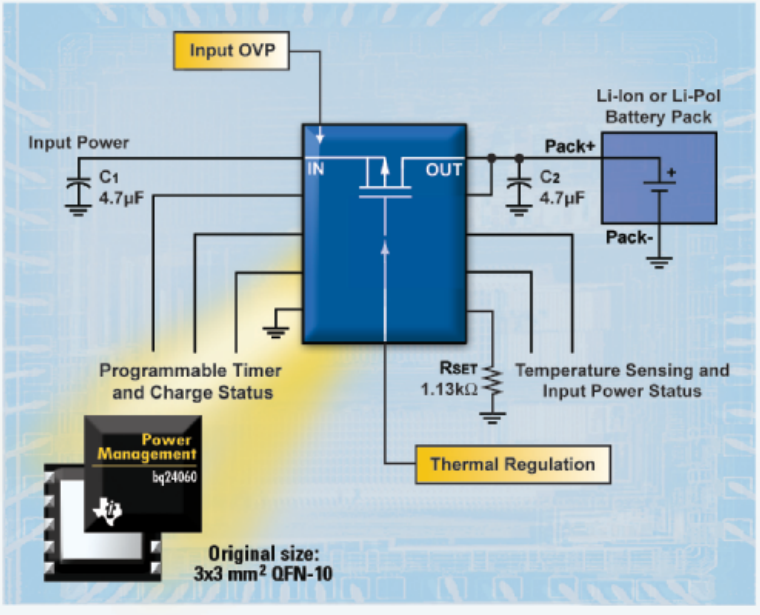
POWER MANAGEMENT

Safer, Faster, Cooler Charging

1-A Single-Chip Li-Ion Charger with Thermal Regulation



▶ Applications

- Smartphones, PDAs
- Bluetooth headsets
- MP3 players
- Digital cameras
- Handheld devices

▶ Features

- Over-voltage protection
- Thermal regulation
- LDO mode operation
- Integrated charge FET, reverse leakage protection and current sensor
- Price: $1.20 in 1k units

The new **bq24060** highly integrated Li-Ion and Li-Pol linear charger IC from Texas Instruments is ideal for space-limited portable applications. It offers a variety of thermal regulation and safety features, including over-voltage protection. Additionally, the bq24060 can be configured in LDO mode to power the system when the battery is absent.

TI Battery Charging IC Solutions:

Linear Chargers					
Device	**Li-Ion**	**Input Voltage (V)**	**Charge Current (A)**	**Charge Termination**	**Package**
bq24080	1-Cell	4.5 - 6.5	1	Min. Current and Timer	3 x 3 QFN-10
bq24060	1-Cell	3.5 - 16.5	1	Min. Current and Adj. Timer	3 x 3 QFN-10
bq24030	1-Cell	4.35 - 16	1.5	Min. Current and Adj. Timer	3.5 x 4.5 QFN-20
Switch-Mode Chargers					
Device	**Li-Ion**	**Input Voltage (V)**	**Charge Current (A)**	**Charge Termination**	**Package**
bq24105	1-, 2-, 3-Cell	4.35 - 16	2	Min. Current and Adj. Timer or Host Controlled	3.5 x 4.5 QFN-20
bq24721	3-, 4-Cell	0 - 24	7	Host Controlled through SMBus	5 x 5 QFN-32

Power Management Selection Guide
Datasheets, Samples and Evaluation Modules

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Texas Instruments

Model-based DFM platform emerges

EDA start-up Clear Shape Technologies, the worst-kept secret in the DFM (design-for-manufacturing) market, in November formally announced itself and its two DFM tools. In 2003, industry veterans Atul Sharan, Yao-Ting Wang, and Fang-Cheng Chang, respectively chief executive officer, chief technology officer, and vice president of engineering, founded the company with the idea that advanced process technologies at 65-nm and smaller processes will require model-based physical verification, not just rule-based DRC (design-rule checking). "We've been around for three years now and haven't announced ourselves until now because DFM requires complex engagements," Sharan says. "You have to get validated in the fabs and create a tool that is production-ready."

Indeed, the three largest fabless companies offering 65-nm technologies—TSMC (Taiwan Semiconductor Manufacturing Co, www.tsmc.com); UMC (United Microelectronics Corp, www.umc.com); and the common process alliance of Chartered Semiconductor (www.charteredsemi.com), IBM (www.ibm.com), and Samsung (www.samsung.com) have endorsed Clear Shape's tools. Qualcomm (www.qualcomm.com), NEC (www.necel.com), and an unnamed company are currently using the tools. The unnamed entity is likely ATI (www.ati.amd.com), which Clear Shape quotes in its press materials.

Sharan says that, although most vendors offering DFM tools claim that IC designers are using their tools, most tools find use with mask-data-prep engineers, mask makers, or the foundries themselves. Sharan notes that many of the "DFM companies" that Synopsys (www.synopsys.com), Cadence (www.cadence.com), and Mentor (www.mentor.com) acquired last year fix OPC (optical-proximity-correction) and PSM (phase-shift-mask) tools in the mask-making process. Clear Shape's tools, according to Sharan, are true DFM tools, because they bring process models of lithography, RET (resolution-enhancement technology), OPC, CMP (chemical-mechanical polishing), mask, etch, interconnect parasitics, and transistor modeling to physical design and verification to help IC designers ensure that the fab they are targeting can manufacture their designs.

Clear Shape based its tools on a patent-pending, model-based, nonlinear optical-transformation algorithm. "We give the designer the ability to go from ideal GDSII [Graphic Design System II] to actual predictive-silicon-based design," Sharan says. "We've created a platform to essentially manage all aspects of variability as they effect design. The primary causes of variability arise from the technology or process issues from the process side." He says that designers must comprehend those issues and then account for those for variability on every axis: timing, leakage power, signal integrity, and catastrophic failures.

The Clear Shape platform currently includes the OutPerform and InShape tools. Cell, IP (intellectual-property), custom-analog, and cell-based digital designers can use OutPerform during physical design. Cell-based-chip designers input their DEF (Data Exchange Format), SPEF (Standard Parasitic Exchange Format), library information, and fab-DFM technology files into OutPerform. The tool then identifies timing- and leakage-parametric hot spots for violations due to systematic variations. The tool also calculates the change in delay and timing skew based on the in-context shape variations and provides delay variations back to static-timing-analysis tools in the form of an incremental SDF (Standard Delay Format).

For custom and analog flows, users feed the tool a Spice netlist and Spice models. The tool then predicts current density across channels, extracting transistor parameters for transistors from the embedded InShape-model-based silicon-contour-prediction engine. The tool then produces a back-annotated-transistor-Spice netlist and applies the changes in RC data to the designer's existing DSPF (Detailed Standard Parasitic Format) or SPEF file to represent the true effects of in-context silicon-shape variations without creating new nodes or parasitic elements. Designers can then simulate the back-annotated-transistor-Spice netlist with their Spice simulators to check the effect of variations on their designs and detect potential failures before going to silicon.

InShape is, in effect, a full-chip DRC/LVS (layout-versus-schematic) checker, which catches the problems that rules-based tools can't, according to Clear Shape. Whereas DRC and LVS tools confirm that a design conforms to an ever-growing set of foundry rules for a given process, InShape checks each layer of a design to ensure that elements conform to actual fab-process models.

Rules-based engines apply an ever-growing list of rules across an entire design and do not account for in-context or situational issues that may impact every design, says the company's vice president of marketing, Nitin Deo. "In the absence of knowing what the design is going to look like, you can have a design that is DRC-clean, but what you get is silicon that encounters catastrophic failures and parametric failures," Sharan says.

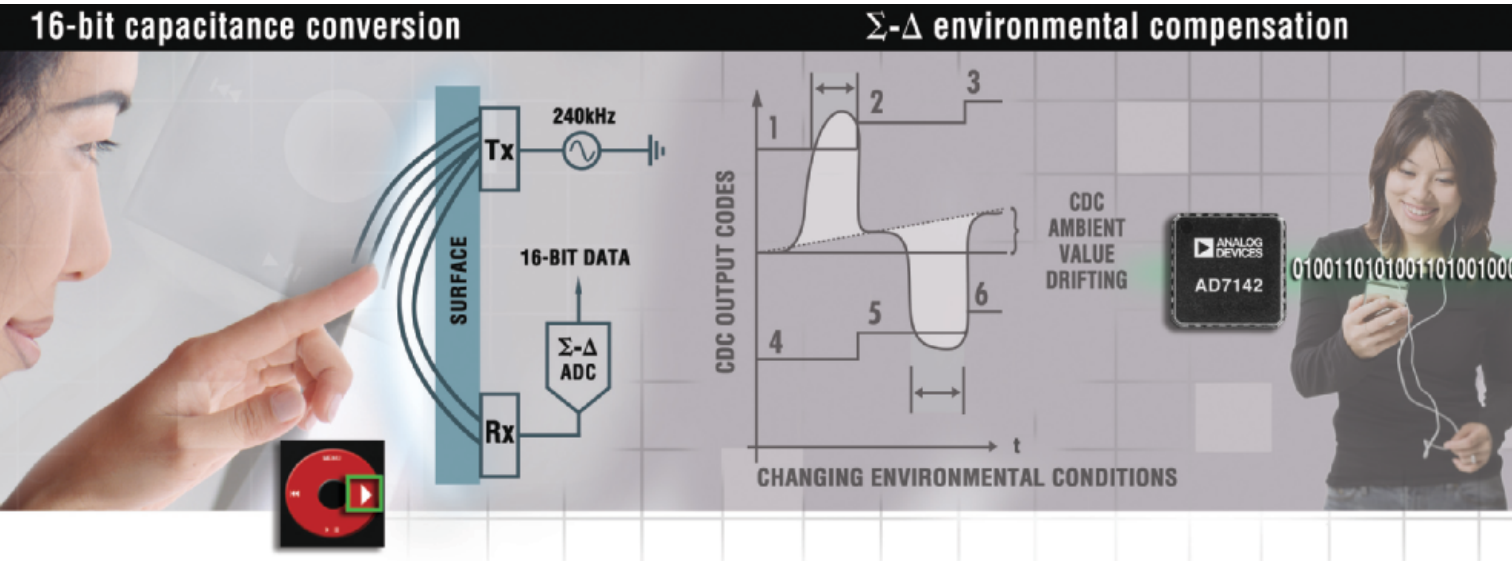
During physical verification, designers use InShape to scan their entire design—both device and interconnect—to identify structures that will later cause problems in RET, OPC, mask, etch, and lithography. The tool then automatically generates a set of "fixing guidelines" that designers can use to implement changes in third-party place-and-route tools. The tool can also produce a critical dimension report that designers can feed into OutPerform.

Sharan stresses that the tool doesn't create rigid guidelines; rather, it produces a DFM-hotspot list and ranks issues—opens and shorts, contact coverage, gate variability, and line-end pullback in the designers' original layout—by type and criticality. Designers can also use the tool's contour-prediction features to do what-if analysis. Prices for OutPerform and InShape start at $300,000 each per master license per year.

—by Michael Santarini

▷**Clear Shape Technologies**, www.clearshape.com.

16-bit touch controller for the best user experience.
In data conversion, analog is everywhere.

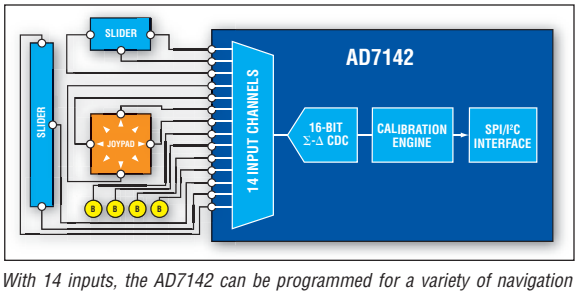


16-bit Σ-Δ CDC …

- <1 femtofarad resolution
- Full power mode: <1 mA
- Low power mode: 50 μA
- Shutdown current: <2 μA
- Supply voltage: 2.6 V to 3.6 V
- Automatic environmental calibration
- Automatic adaptive sensitivity
- SPI® or I²C® interface
- 32-lead 5 mm × 5 mm LFCSP
- Price: $1.65 (1k quantities)

… enabling multiple applications

- Consumer electronics
- Medical instrumentation
- Automotive applications
- Industrial equipment
- PC peripherals



With 14 inputs, the AD7142 can be programmed for a variety of navigation functions including buttons, sliders, scroll wheels, and joypads.

Improved sensitivity and environmental calibration—made possible by Σ-Δ conversion

For products with increasing feature convergence, finger-driven navigation enhances the user experience—for designers as well as consumers. The AD7142 capacitance-to-digital converter (CDC) with on-chip environmental compensation delivers unmatched touch control performance. It offers:

- Reliable performance over supply and temperature
- Programmable functionality and touch sensitivity
- 50% lower power than competitive solutions
- Development tools, such as reference designs and host software, that reduce time to market

ADI also offers CDC solutions for measuring proximity, position, level, pressure, and humidity.

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ANALOG DEVICES

VOICES

Cherokee International: Where in the world are design and manufacturing?

When electronic-hardware companies perform research on where to build manufacturing facilities, they must consider more than just which country has the cheapest labor rates. In this brave new world of electronics design and manufacturing, concerns such as a country's technology, supply-chain infrastructure, point of consumption, and flexibility are equally important.

Cherokee International (www.cherokeepwr.com), a vendor of ac/dc- and dc/dc-power supplies, is no neophyte to offshore manufacturing: With its headquarters in Tustin, CA, Cherokee has design centers and manufacturing throughout the world. Tustin, CA, and Wavre, Belgium, are design centers and manufacturing locations for high-volume, low-mix quantities. Cherokee's Guadalajara, Mexico, facility has in the past handled the company's higher volume products, and its facility in Bombay, India, has long manufactured its magnetic components. Recently, Cherokee underwent a re-evaluation of its operations, so it performed a global analysis of where to locate its next generation of manufacturing and design. At first glance, Mexico seemed the logical place to expand design and manufacturing. However, considering proximity to the customer, the opportunity to call on the Asian market, and other factors, Cherokee decided to build in Shanghai, China. *EDN* asked Mike Wagner, vice president of marketing and an electrical engineer who started out as a power-supply designer, what led to Cherokee's change of manufacturing strategy.

Why did you look at moving manufacturing from Mexico? Aren't Mexico's labor rates among the lowest in the world?

A Yes, Mexico has low labor rates—not the lowest—but there are other important factors to consider, and Mexico just didn't come up on top when we factored in the other aspects.

So, if labor rates alone weren't the determining factor, what were the other key influencers? They must have been significant, because you already had an operating facility in Mexico.

A In addition to point of consumption and supply-chain location as two main issues, we also made a consideration for finding engineering talent that could support a future design center. Also, more North American and European customers today are doing their system integration for their end products in China. Finally, we expect to call on the Asian market, which is growing considerably. We believe that Asia will become a significant consumer of our power supplies.

Was China a slam dunk relative to labor rates, then?

A Actually, no, because China's labor is not the lowest priced. For example, India has marginally lower labor rates.

Why not build in India, which has a famously excellent engineering-education system, and, besides, you had some infrastructure there already?

> "Analog expertise is the key. ... China is a self-contained system of engineering, parts, labor, and customers.

A Yes, but India's educational strength is more known for software engineering rather than analog engineering. China has a much stronger power-engineering educational system, and analog expertise is the key. Plus, we don't see India's being nearly as robust a customer in the future for power-supply consumption. India also doesn't really have an electronics-supply chain. So, if we were to manufacture power supplies in India, we would have had to pay to ship materials from China to India for manufacturing, and then we'd have to pay added freight and duty to ship the finished product back to the end customer in China. China is a self-contained system of engineering, parts, labor, and customers.

Building a facility is always a gamble. Why didn't you go with CM (contract manufacturing) and sort of ease into manufacturing there?

A We've avoided CM because we feel that we can better control our quality by having common processes, equipment, and training across all our facilities. That way, we own the entire manufacturing process and do not depend on a CM whose schedule is fluctuating and subject to other customers the CM supports.

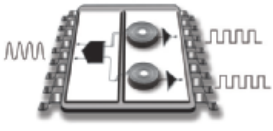
How do US engineering costs compare?

A Chinese engineers cost about a third of US engineers, but the higher priced US engineers also have higher level skills sets, at least for now. **—by Margery Conner**

Isolation and innovation in one package.
With *i*Coupler technology, analog is everywhere.

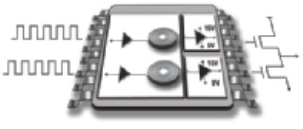
*iso*Power™ Technology

- ADuM524x family
- 50 mW isolated, regulated power
- Two data channels
- 2.5 kV data isolation
- Starting at $2.95



Converters

- AD740x family
- Industry-leading converters with integrated isolation
- 16-bit, 10 MSPS, 3.75 kV isolation
- Starting at $4.00



Gate Drivers

- ADuM1230
- Dual gate driver, 100 mA drive, 2.5 kV isolation
- High side isolated from low side
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Communications

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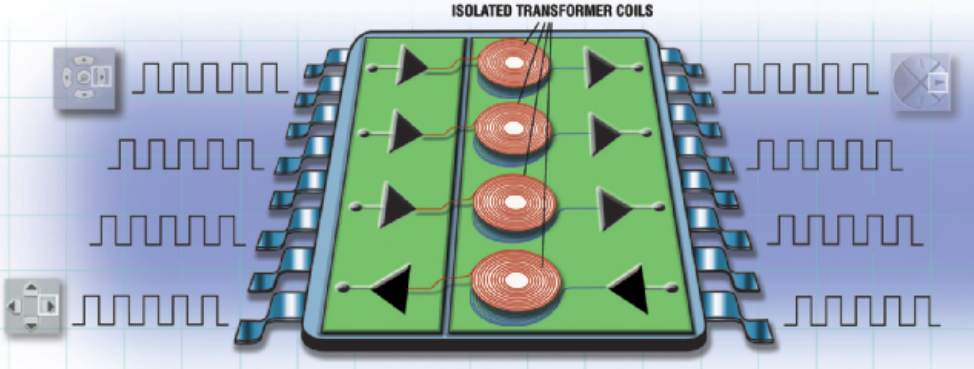

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ANALOG DEVICES

BY BONNIE BAKER

Comparing DAC architectures

Entry-level engineers know ADC topologies so well that during interviews, most job seekers can draw and explain fundamental block diagrams. The same situation does not hold true for DAC topologies. In this case, applicants can tell me only the basics: Digital goes in, and analog comes out.

DACs you find in high-precision control-loop applications typically use the R2R (resistor ladder) MDAC (multiplying DAC, **Figure 1a**). This architecture can achieve high-voltage output. MDAC manufacturers can design high-resolution (16-bit) devices with ±1 LSB INL (integral-nonlinear) and DNL (differential-nonlinear) specifications. MDACs require an external current-to-voltage operational amplifier but exhibit fast settling time (less than 0.3 µsec) with a multiplying bandwidth that can be greater than 10 MHz.

The R2R-back DAC is most appropriate for industrial applications (**Figure 1b**). With this DAC, each update involves switching the 2R legs to either the voltage reference high, V_{REF-H} or the voltage reference low, V_{REF-L}. This architecture can be relatively simple to manufacture. The R2R architecture has a parallel data-input bus. For devices with a serial interface, the multibit DAC uses a serial-to-parallel register internally before latching the data to the DAC. In either case, gate-switch timing skews manifest themselves at the DAC's output as glitches. The R2R-back DAC, like the MDAC, typically has excellent low noise, INL, and DNL performance, with medium settling-time capability.

The string DAC suits portable-instrumentation, closed-loop-servo-control, process-control, and data-acquisition systems (**Figure 1c**). The **figure** shows a model of a 3-bit-resistor string DAC. Here the digital-input code is 101b, which decodes to $5/8V_{REF}$. The output-stage buffer isolates the internal resistive elements from the output load. The string DAC is a low-power option that guarantees monotonicity with good DNL performance across the input-code range. The glitch energy is typically lower than that with other types of DACs; however, the INL performance is sensitive to chip layout and depends on resistive-array matching. The noise of string DACs is also relatively high and again depends on the resistive-string-array impedance. EDN

Bonnie Baker is a senior applications engineer at Texas Instruments. You can reach her at bonnie@ti.com.

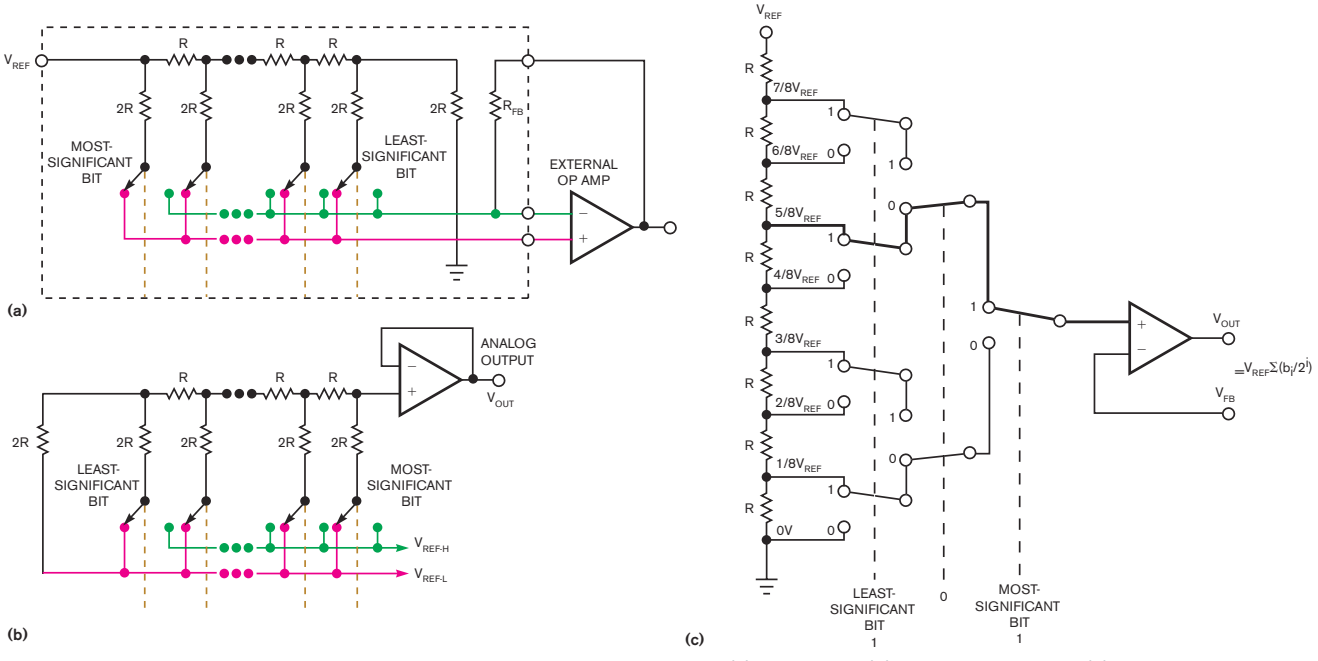

Figure 1 Typical topologies of popular DACs include R2R-multiplying (a), R2R-back (b), and resistor-string (c) architectures.

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One man's trash …

DANIEL VASCONCELLOS

I took a consulting job with a major semiconductor-equipment-manufacturing company. There, I built various test fixtures using surplus VMEbus-card cages that the company had in the warehouse. It was great to be able to get almost the same card cage that the company was shipping in the current product. One day, I found myself requesting another card cage for a new test fixture. The guy in the warehouse told me that I had better grab any other card cages now, because they were all going to be "in the dumpster" the following week. They needed the space in the warehouse. I protested; guys like me needed them for important company projects. I suggested that I would be interested in buying them; my real goal was to get someone to realize they were tossing out something useful. I was asked to bid on them. I didn't want them, so I put in a low bid of $100.

Two weeks later, I had forgotten about the VMEbus-card cages. Then I got the call. A voice droned, "You are the successful bidder on lot number 13285. You have 48 hours to get the nine pallets out of the warehouse." I felt panic, thinking, "My wife is going to kill me. Where am I going to put these things?" I had an addition to my house that was framed and roofed but unfinished inside. I thought that I could store them there for a short time to keep them out of the rain. If nothing else, I could burn the oak pallets to heat my house.

I made a deal with my wife that I would sell them all in six weeks or drive them to the dump. I created a flyer that described the item and showed the purchase cost of all of the components and included a photo. It came to $845 each, so I set the "sale price" at $250. I found a trade magazine that specialized in the VMEbus. I sent a letter to every company mentioned in the magazine. It worked. The orders started flowing in. In fact, the only resistance to purchase seemed to be, "Why are you selling them *so cheap*?" Instead of telling them that "my wife was going to kill me if I didn't get rid of them," I said something like "we are overstocked and eager to move them out at a low price."

Orders for one unit were followed by orders for multiple units. I was feeling much better about my "impulse buy." The kicker came when I got a frantic call from a purchasing agent from the same company from which I had originally obtained the nine pallets. One of the company's engineers had put in a request to purchase four units. This request represented sweet vindication for me; I sold him back those four units for 10 times what I had paid for all nine pallets!

About two years later, I got another consulting assignment at the same company. The company set me up to do my rush project development in a storage room. One day, I asked a guy about some items that were stacked against a wall, how much they were worth, and why no one was using them. That was a lot of money sitting there! I suggested the company assign someone to go around and sell off these idle assets. The guy told me a story. He had heard of a consultant who had bought about 100 pallets of surplus VMEbus-card cages and sold them for about a million dollars. I felt my face grow warm as I realized that he was talking about me, but the numbers were greatly exaggerated. I did make approximately $20,000, but it sure did take some work, and there was the real risk that my wife would toss me out to sleep with the racks. I don't know if I had anything to do with it, but the company finally took my advice and created a department to dispose of surplus equipment in a more orderly fashion. EDN

Marty McGrath is an electronics and software-design consultant at McGrath Technical Services (Sunnyvale, CA). Like Marty, you can share your Tales from the Cube and receive $200. Contact Maury Wright at mgwright@edn.com.

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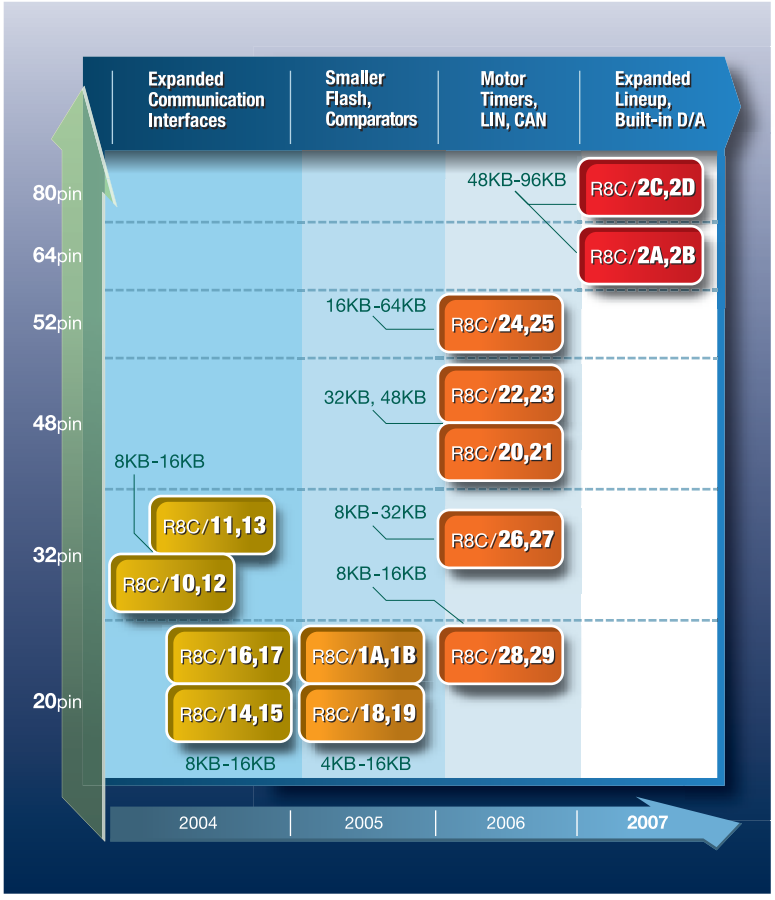
R8C/Tiny Product Roadmap



HOT Products | **R8C/25**

R8C/Tiny CPU	Program Flash (16KB - 64KB)	RAM (1KB - 3KB)
Oscillation Circuit Main Clock (20MHz Max.)	Data Flash (2KB)	Power-On Reset Circuit
On-chip Oscillators (40MHz, 125KHz)	Low Voltage Detect Circuit	Protect Register
Oscillation Circuit Sub Clock (32KHz Clock)	Enhanced WDT	16-bit motor control Timer (2)
RTC	External Oscillation Stop Detection	8-bit Timer (3)
Serial I/O Clock Sync./ UART (2ch)	SSU/I2C	A-D Converter (10-bit x 12ch)
44 GPIO	Hardware LIN	On-Chip Debug

Package: 52pin LQFP (10mm x 10mm, 0.65mm pitch)

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- **Scalable**
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  - Includes 40MHz on-chip oscillator, data flash, power-on reset circuits, several 8- and 16-bit timers, up to 20 channels of A/D, D/A, LIN, CAN and more
- **Reliable**
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  - Watchdog timer with on-chip oscillator, programmable low-voltage detect circuit
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  - Complete software and hardware tools for short development cycle
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*Source:Gartner Dataquest (April 2006) "2005 Worldwide Microcontroller Vendor Revenue" GJ06333

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Seeking the secrets of a satellite receiver

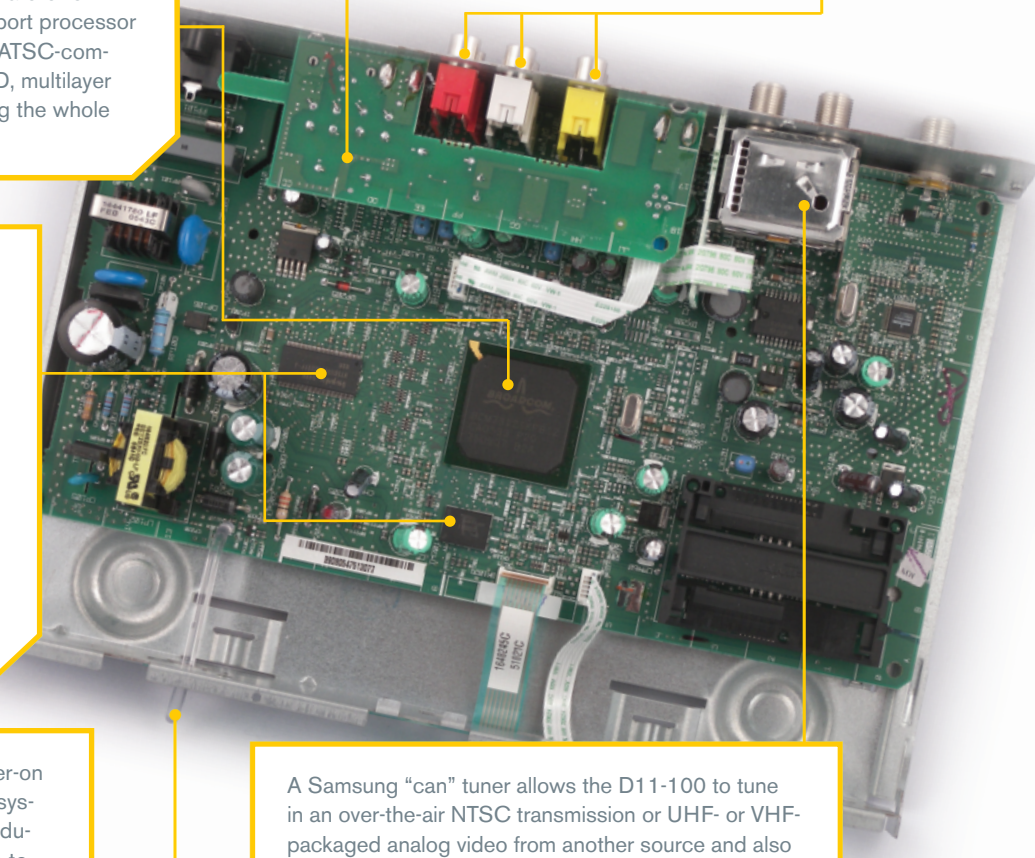
DIRECTV SET-TOP-BOX DESIGN FOCUSES ON MODULARITY FOR THE MASS MARKET.

Rendered redundant by the acquisition of a more advanced unit, a DirecTV D11-100 satellite-set-top box gets the Prying Eyes treatment for your voyeuristic enjoyment. Peer inside the svelte, silver case to see how the box's creators used modularity to make a common base design amenable to multiple markets.

The multimedia-processing heart of the D11-100 is a Broadcom BCM7312—a single-chip, satellite-set-top-decoder IC that integrates an RF tuner; an all-digital, variable-rate receiver with 7-bit ADCs and an FEC (forward-error-correction) decoder; a data-transport processor with security capabilities; MPEG-ATSC-compliant audio/video decoders; a 2-D, multilayer graphics engine; and, coordinating the whole show, a 266-MHz MIPS32 core.

Analog-modem hardware, which allows the D11-100 to periodically dial home for program-guide, firmware, and other updates, also resides on a separate daughtercard.

Given all the attention to design efficiency elsewhere, the inclusion of two sets of composite audio/video outputs is baffling. Because the unit has only one tuner and one decoder, the outputs can't deliver separate programs. So, why did DirecTV shoulder the additional hardware cost? (Go to www.edn.com/070118pry for some speculation and to post your own thoughts.)



The memory subsystem includes a Hynix 256-Mbit DDR SDRAM and a BGA-packaged device with an "FW603" firmware code and handwritten "FT" (firmware tested?) initials on its top. Because DirecTV set-top boxes are field-reprogrammable, it's likely that the BGA device is at a minimum a single-die flash memory. It might also be a dual-die flash memory with redundancy to enable a fail-safe upgrade methodology or a combination of SRAM and flash memory.

A clever "light pipe" routes power-on illumination from an LED on the system board to the front panel. Modularity allows the D11-100 design to morph to suit the varying cosmetic tastes of multiple markets through the use of interchangeable front panels.

A Samsung "can" tuner allows the D11-100 to tune in an over-the-air NTSC transmission or UHF- or VHF-packaged analog video from another source and also broadcasts the outgoing RF video on VHF channel 3 or 4. The device is on a modular daughtercard, suggesting that lower cost boxes using the same base design might not include the RF video-input feature.

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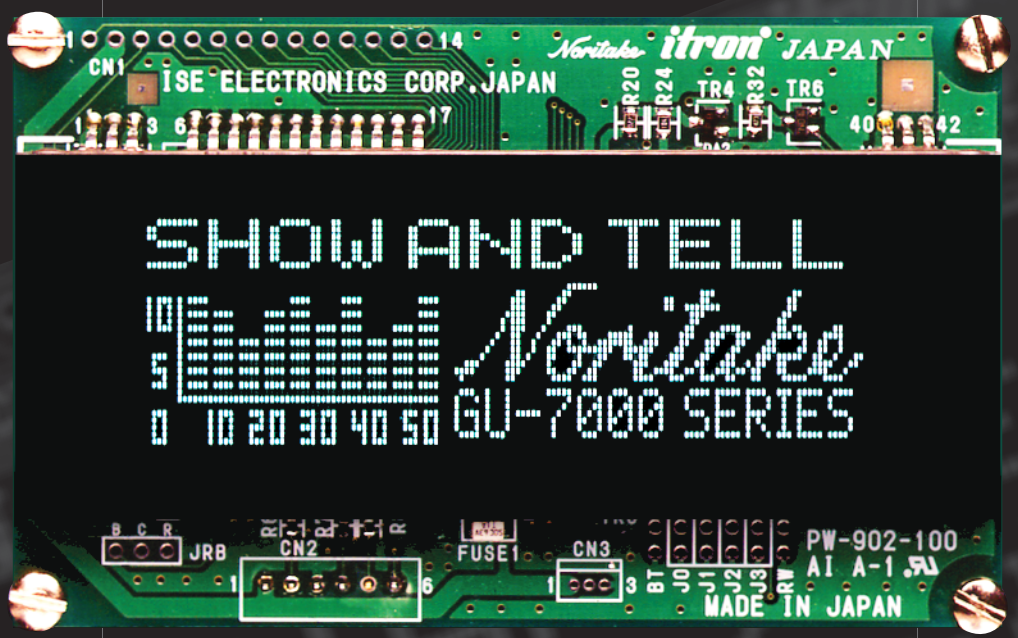

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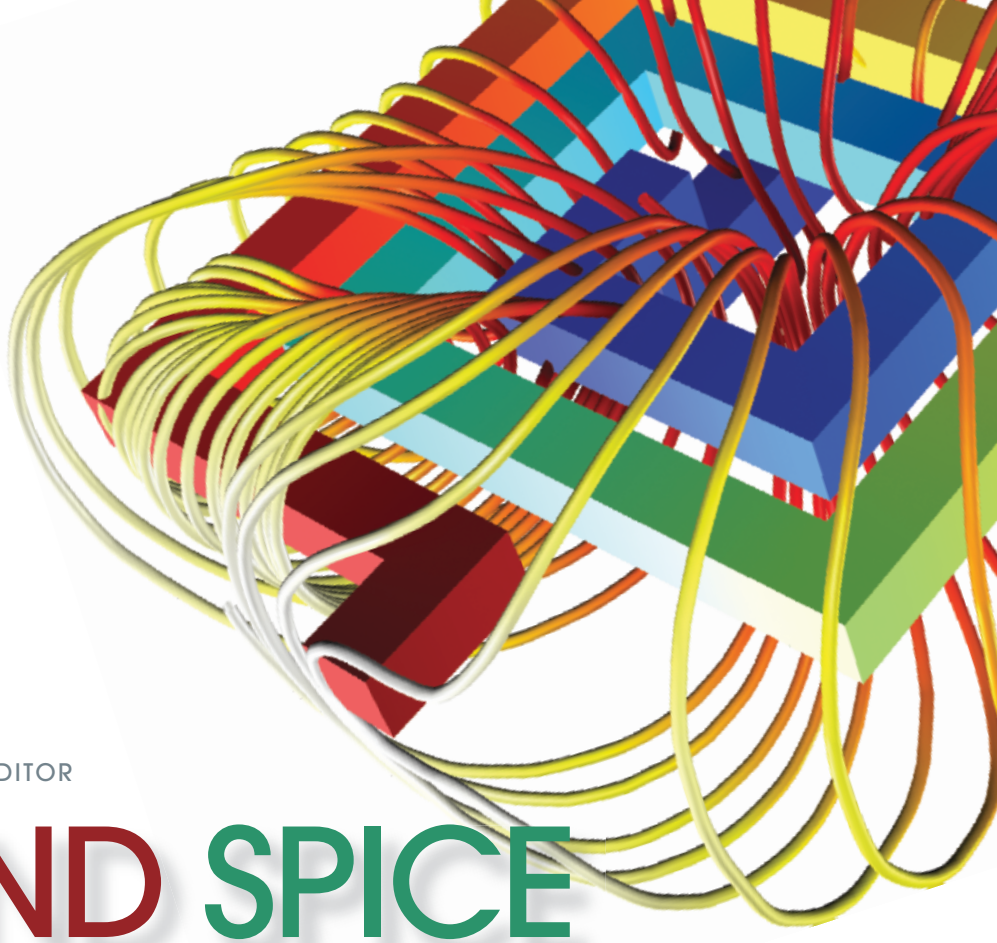


FIELD-SOLVER SOFTWARE CAN PREDICT THE BEHAVIOR OF CIRCUITS THAT OPERATE AT SPEEDS AND DENSITIES BEYOND THE CAPABILITIES OF SPICE TO PROPERLY MODEL. WHETHER YOU ARE TRYING TO VERIFY SIGNAL INTEGRITY OR DESIGNING AN RFIC, YOU SHOULD KNOW HOW FIELD SOLVERS COULD HELP YOUR DESIGN.

BY PAUL RAKO • TECHNICAL EDITOR

BEYOND SPICE

Spice is a popular circuit simulator. As electronic designs move to higher frequencies and occupy less space, Spice is often insufficient to predict the behavior of even simple circuits. When this scenario occurs, engineers must turn to the use of field-solver software. Field solvers, sometimes called EM (electromagnetic)-field solvers, calculate Maxwell's equations for a physical representation of your circuit (**Reference 1**). You must provide the field solver with a representation of the physical configuration of the circuit, which you base on the output of either an IC- or board-layout package or a solid model. The solid model also must include the properties, such as resistance and dielectric constant, of all the materials in the area of interest. **Figure 1a** shows the modeling of a transmission line, and **Figure 1b** shows the resultant field distribution. Note that field solvers do not solve the quantum-mechanics problem of what occurs in transistors or other active devices. Field solvers instead focus on traces, inductance, capacitance, and the way these devices interact.

SPICE AND ITS LIMITATIONS

The Spice software tool tries to predict the performance of electronic circuits. It works in the time domain—that is, it solves for the voltage and current at small, discrete time steps and then displays a transient simulation, which looks similar to an oscilloscope trace. When you want a frequency response, it solves the time-based problem at a set of frequencies and displays the result as a Bode Plot. The best explanation available for the operation of Spice is *Inside Spice: Overcoming the Obstacles of Circuit Simulation* (**Reference 2**). **Reference 3** provides a good online summary of Spice. Spice is famous for the headaches it can cause design engineers (see **sidebar** "The trouble with Spice").

Note that Spice does not solve for physical things, such as board layout and signal interactions. The schematic has no data to convey that information; it is simply a collection of lumped elements and subcircuits. The vagaries of Spice output became clear 15 years ago when not one of five Spice programs agreed with the performance of the actual circuit (**Reference 4**). Spice does have transmission lines and sometimes even lossy transmission lines. These lines represent a lumped-element subcircuit with a parameter to account for the length of the line. Spice does not base the calculation of the lossy characteristic on the layout but simply accounts for it in a formula that bases the prediction of losses on simple parameters. Spice also fails to model physical phenomena, such as skin effect, although lumped-element subcircuits can approximate these phenomena (**references 5** and **6**).

Field-solver programs, which can model physical phenomena, now enter the picture. Thomas Quan, vice president of marketing for Applied Wave Re-

search, notes: "As operating frequency increases in analog circuits, analog designers will benefit greatly from employing high-frequency-design techniques and tools that have been in use by microwave designers for many years."

A field solver calculates how a stripline or spiral inductor will act. The user enters a virtual representation of the device as a solid model. This solid model can come from a layout package, or the user can draw it using the field-solver program itself. Many field solvers accept solid models from mechanical-CAD software such as Solidworks and Unigraphics. In addition to the physical shapes of the circuit elements, the field-solver software must know the electrical properties of the material the design uses. This requirement includes not just the conductance of copper and aluminum, but also the dielectric constant of the pc board, glass oxide, or solder mask that is near the conductive elements. At the extreme, the solid model could include the glass fibers inside an FR4 pc board as well as the solder-mask marking that may lie on top of a trace. The IC model could include not just the glass oxide on which you place a spiral inductor, but also the metal layers underneath and the epoxy that encapsulates the die in a finished package. For designs operating at high frequencies, all these factors will matter in how the circuit behaves.

Spice creates a conductance matrix from a circuit netlist and attempts to solve that matrix over various time steps. Field solvers use meshing techniques, much like finite-element-analysis programs for mechanical stress and strain. Once the software meshes the virtual physical representation into small elements and the user provides the dielectric constant and conduction of those elements, the field-solver program uses various mathematical techniques to deduce the fields and, hence, voltage and currents that are associated with the circuit element. You should remember the admonishment of Henry Ott, a noted authority on signal integrity: "Remember: Fields make currents, not the other way around."

When the field solver has examined the physical representation of the circuit, it can then output an electrical representation of that configuration as either an S-parameter or LRGC (inductance/resistance-conductivity/capacitance) model. The S-parameter model is a frequency-domain representation, and the LRGC model is a representation for time-domain analysis by Spice engines. Even if there is only an S-parameter output, programs can perform a mathematical convolution to achieve an inverse-Fourier transform. This step gives a time-domain representation of the network more suitable for solution in Spice, although at a risk of inaccurate results.

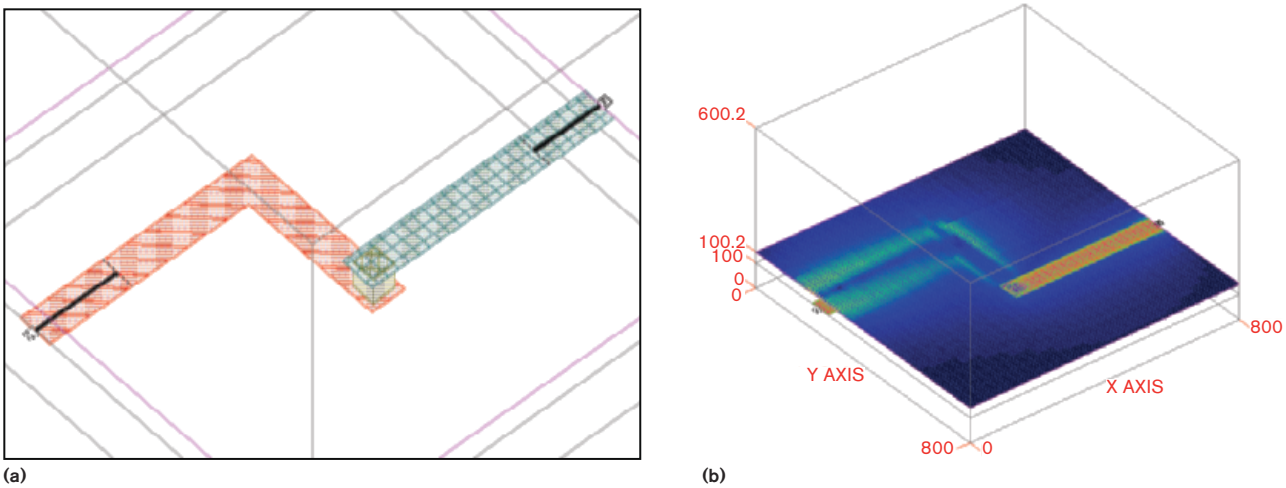
AT A GLANCE

- Spice cannot accurately solve high-speed or small, interacting circuits.
- Field solvers calculate Maxwell's equations for any passive circuit.
- Field solvers provide time- or frequency-based data to a simulator.
- Modern simulators can solve in the time or frequency domain.
- You use field solvers for signal-integrity and RF design.

FIELD-SOLVER SHORTCOMINGS

On the downside, field solvers can cause several design problems. The field solver must use an adequate mathematical method for the proposed problem. If you use a 2- or 2.5-D solver in designs having 3-D fields, then expect to be suspicious of the answer the field solver produces. As always, the universal software problem of garbage-in/garbage-out also arises. If you incorrectly model the structures or incorrectly enter the dielectric constant or other properties, then the field solver is hardly to blame when you get inaccurate answers. There are also sophisticated mathematical problems that may not be a function of the field solver itself but, rather, how the simulator converts an S-parameter frequency-domain output from a field solver to a time-domain representation for use in signal integrity or any non-steady-state analysis. Doing a convolution on the S-parameter data performs the inverse-Fourier transform. This transform does the conversion from the time domain to the frequency domain. Rational-fitting algorithms, or state-space equations, may also perform the transformation from the frequency domain to the time domain. Two problems can arise if the algorithms are inadequate for the S-parameter data set: causality and passivity.

If the field solver violates causality, a time-domain model that you generate



(a) (b)

Figure 1 A user can directly model circuit traces, or the layout package can feed back the physical configuration (a). The field solver uses this input (b) to calculate the fields, voltages, and currents (courtesy Applied Wave Research).

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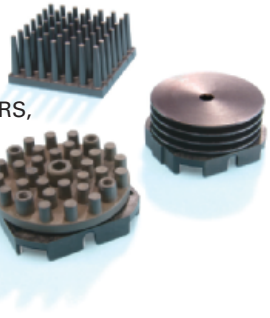

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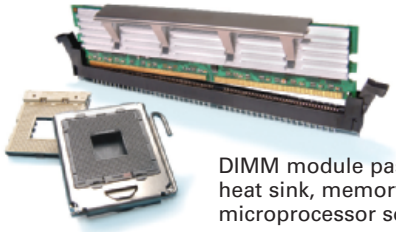

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from the S-parameter data may behave erratically. For example, a negative-going reflection may appear instantaneously when you launch the signal into a trace or a conductor. This behavior means that the model has neglected to account for the finite transit time the wave takes to reach any reflection-causing discontinuity. Problems with causality result in inaccurate results. Passivity arises when the transformation creates a time-domain model that adds energy to the circuit despite the fact that no active devices are in the subcircuit. Problems with passivity cause the simulation to blow up and fail to converge.

These problems involve complicated mathematical algorithms and should remind diligent engineers that they are designing for the real world. Without real-world verification, problems will occur because of too great a reliance on computer simulations. You need three tools to validate field-solver outputs: experience, a VNA (vector-network analyzer), and TDR (time-domain reflectometry).

You should have filed away in your

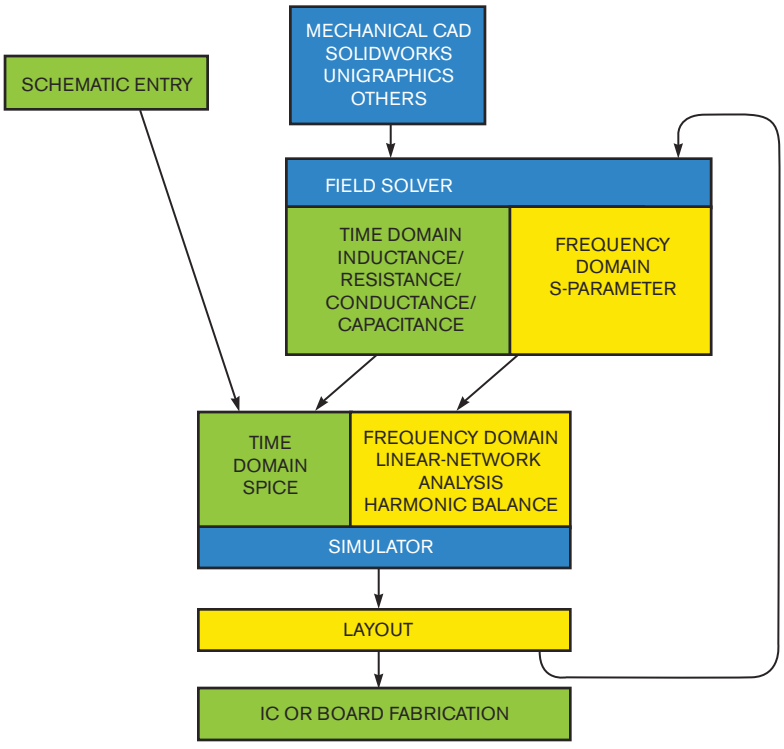

Figure 2 A design flow includes a field solver to better simulate real-world issues, such as board and IC layout or component interaction.

THE TROUBLE WITH SPICE

Spice is a powerful tool that can solve intractable problems. It solves Kirchoff's laws in the time domain. Spice uses matrix math to solve the conductance matrix of the circuit, which the schematic netlist describes. The program iterates from an initial first guess until it gets a result close enough to declare that it is accurate; it then moves to the next time step and repeats the process. Spice models networks of resistors, inductors, and capacitors as simple elements or, better yet, with subcircuits that reflect equivalent series and parallel elements, as well as temperature effects. It models active devices as combinations of passive devices and controlled voltage sources and current sources. It also allows you to insert equations into models to "fudge" for noise and similar effects that are too hard or indeterminate to model.

However, Spice runs into trouble in modeling. The results of Spice are only as good as the models. IC designers swear by Spice, often with disastrous results. Almost all board-level designers have had unpleasant experiences with models. As a result, they are more suspicious of the results and usefulness of Spice. IC designers get to use models that cost tens and even hundreds of millions of dollars to ensure that the Spice model matches the results of the actual transistors and passives in the process. Even with these efforts, temperature or proximity effects often make the first silicon behave unpredictably.

"Spice lies–or fails to tell the truth–all too often," says Bob Pease, staff scientist at National Semiconductor. "Use your head when at all possible. Design using pencil and paper, rather than any simulation. And, no matter what Spice tells you, you do not have to believe it. On the other hand, Spice might tell the truth. But, for you to say that, you have to analyze what the circuit will do all by yourself. Otherwise, how would you know what the truth is?"

Engineers contemplating the vagaries of Spice output must assume that the program will give an output, which is often not the case. Spice must converge on every attempt to solve the conduction matrix and every time step it takes to give a response. The problem is that Spice bases the matrix math on linear solutions, and diodes, just like transistor physics, are not linear. Spice must guess an operating point on the exponential curve that is the diode IV chart. As a result, it often fails to converge when a small movement on the curve in the I or the V axis results in a large change in the other variable. If each subsequent guess the program makes does not result in a smaller error, then Spice returns with the dreaded "failed-to-converge" error. Because this iteration procedure has to occur for each time step, a huge number of chances for nonconvergence exist. When Spice attempts to solve nonlinear-magnetic elements, such as transformers, the convergence problems become even more daunting.

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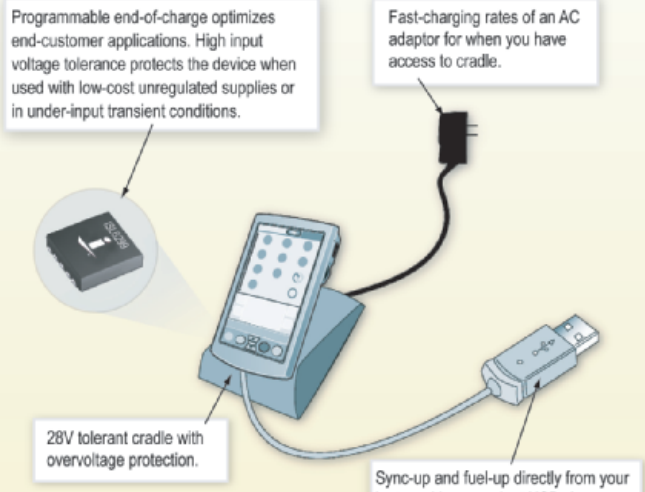
USB input. Takes input from USB port or other low voltage supply. Fixed charge current at typically 380mA. Only charges when cradle source is not connected.



ISL6299A Key Features:

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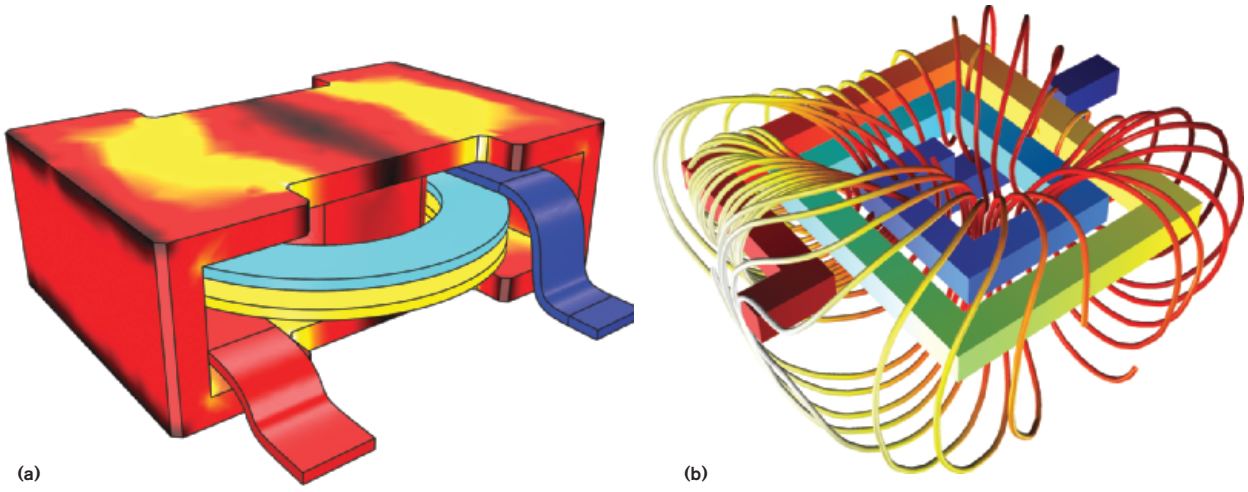

Figure 3 Field solvers can provide results for intractable problems involving nonlinear magnetics (a) as well as complex 3-D spiral inductors (b) (courtesy Comsol).

mind any circuit block, whether on an IC, a board, or a cable, that you have used previously. If the simulator shows a block's acting in an unpredictable way, you should investigate and resolve the conflict. Andy Masto, former vice president of Teledyne CME, performed finite-element analysis starting when the input was a "deck"—of IBM Hollerith cards. "I have never done a single analysis where the answer was right the first time with my initial assumptions," he reports. "There was always a need to evaluate a problem with a known or a simple solution just to verify that the software was acting correctly."

A second technique to check up on your field solver is using a VNA. A VNA

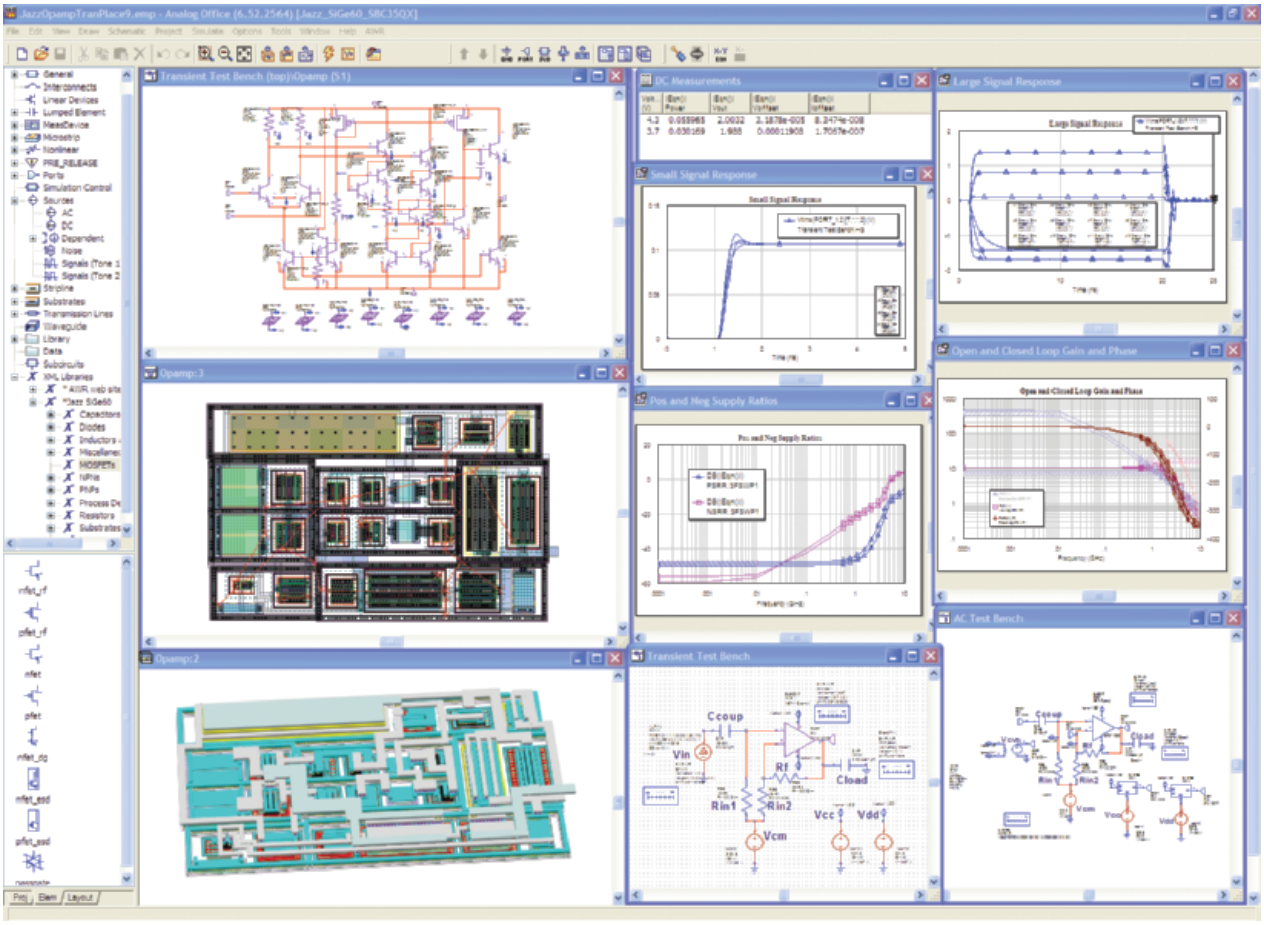

Figure 4 A full-blown design environment allows schematic entry, time- and frequency-domain simulation, layout, and field solvers for signal-integrity and RF design (courtesy Applied Wave Research).

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- Out-of-phase operation to reduce input filter requirements and EMI
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is similar to a spectrum analyzer, but it also records the phase changes of the signal as it passes through a system. By either adding on a separate box or buying an analyzer that has the function built in, the VNA can measure S-parameter data over wide frequency ranges. The 200-MHz, "green-machine" HP 3577A can use the HP 35677A/B to take S-parameter data in 50 or 75Ω systems. For higher frequencies, the 8753ES can work to 3 or 6 GHz and has a built-in S-parameter box. Use caution with instruments such as the Tektronix DSA8200, which does not work like a typical VNA. A traditional VNA sweeps a tuned filter with a narrow bandwidth across the frequencies you are measuring. This technique eliminates out-of-band noise and provides dramatic SNR benefits. The fast DSA8200 scope calculates S-parameters by performing Fourier transforms on a set of time-domain-sampled data to generate frequency-domain results. By its nature, the DSA8200 must be a wideband instrument, meaning that it also has to live with wideband noise, limiting the accuracy of measurements. It would be absurd to use complicated math to convert time-domain data to frequency-domain data, only to have your simulator take the inverse transform to get back to the time domain.

The DSA8200 really shines in TDR measurements. This technique sends a fast rise-time pulse down a transmission line or structure, such as a ribbon cable or another circuit element. It then records the reflections that impedance discontinuities generate. The vertical divisions on the scope when in TDR mode represent impedance, not voltage amplitude. An older tool for TDR measurement is the Tektronix 11801A/B/C series scope with the SD-24 plug-in. Agilent offers the 86100A model, and no discussion of TDR testing should omit the fast-pulse tools from Picosecond Pulse Labs. The company's single-ended 4020 and differential 4022 models set the standard for the industry. The TDR data can run through a program such as Tektronix's (formerly, TDA Systems') iConnect software to generate time-domain Spice models that you can compare with the models that the field solver creates. Note that you can enter data from real-world objects directly into the simulation en-

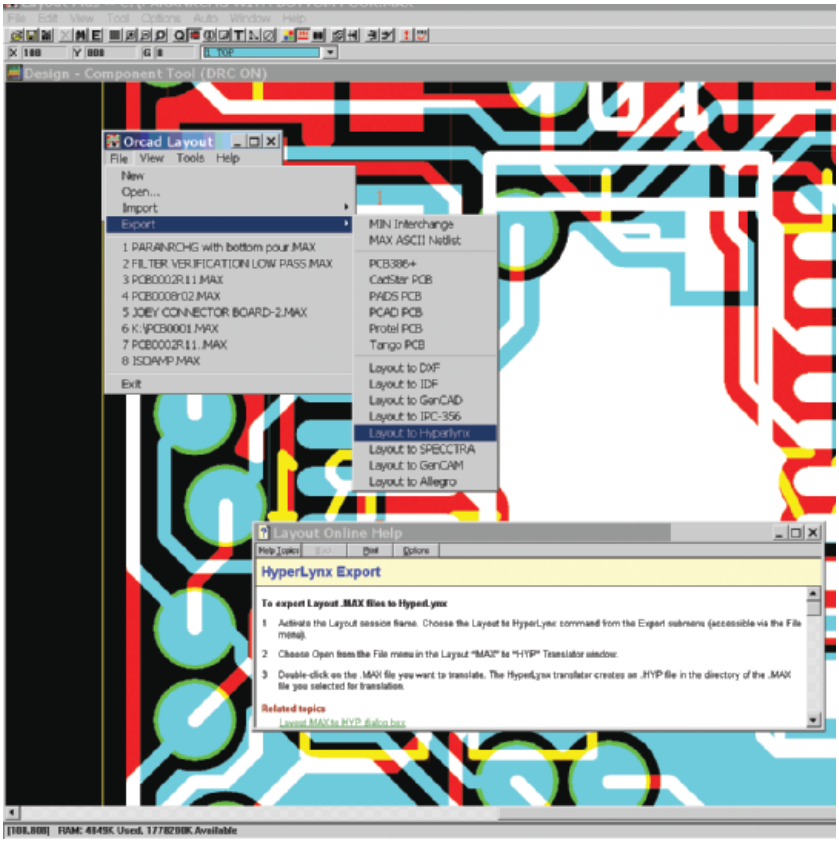

Figure 5 The legacy Orcad layout tool can export to the Hyperlynx file format from the session shell.

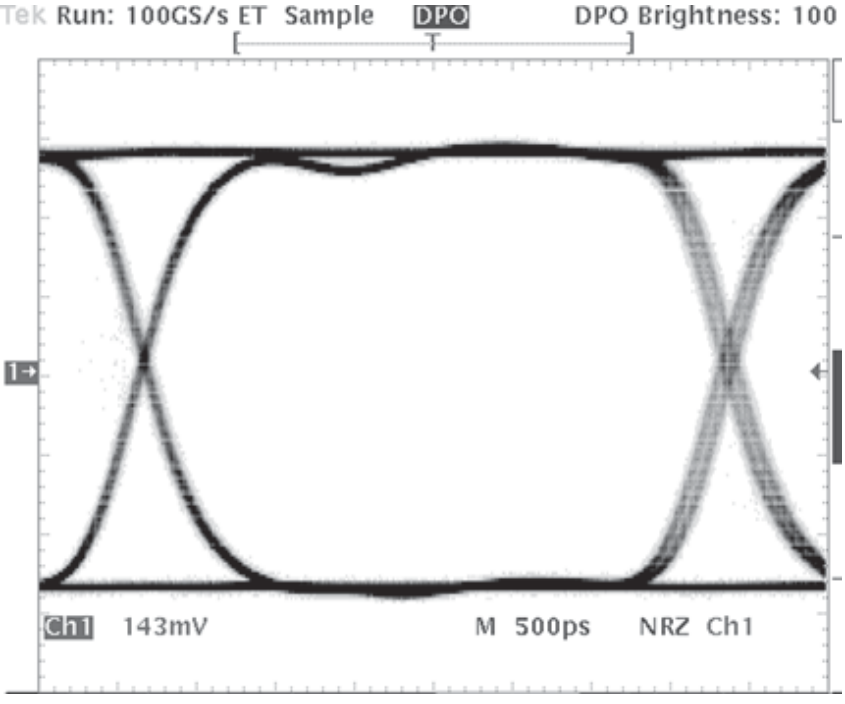

Figure 6 This scope shot shows one eye in an eye diagram (courtesy Tektronix).

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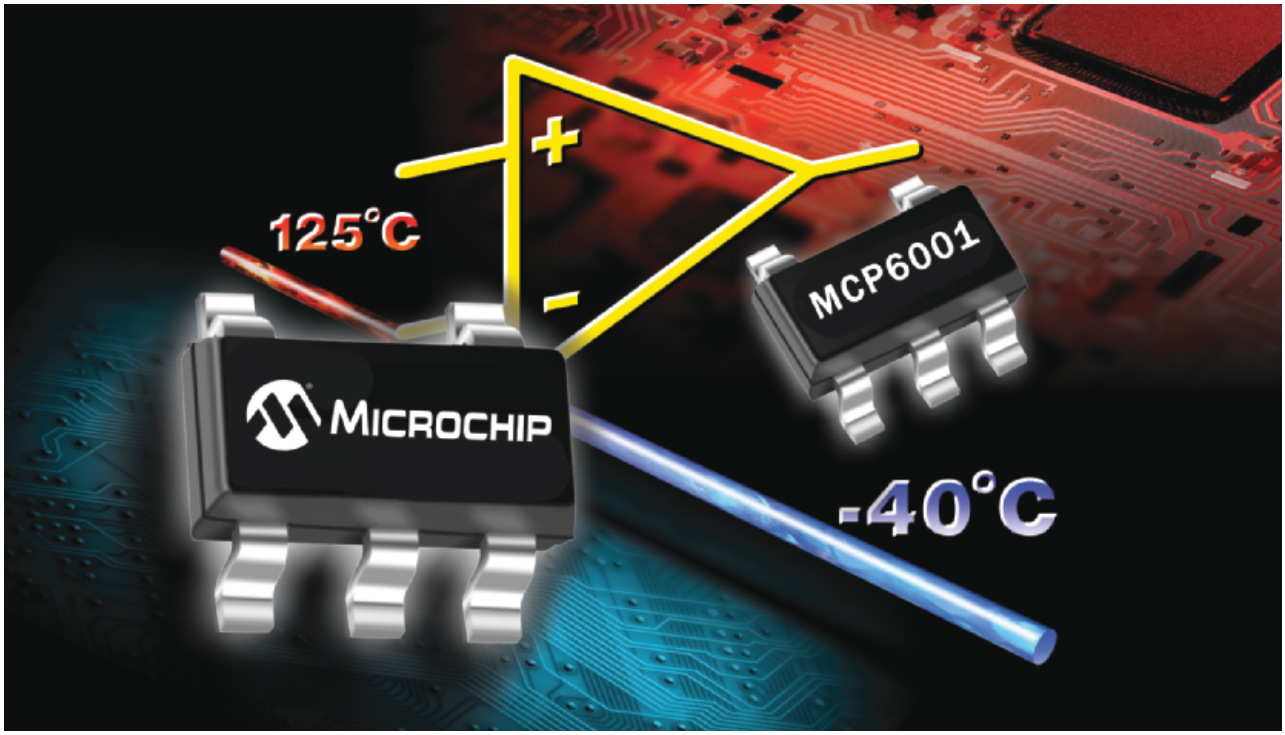

Select Standard Op Amps

Part #	GBWP	Iq Typical (µA)	Vos Max (mV)	Input Voltage Noise Density @ 1 kHz (nV/√Hz)	Operating Voltage (V)
MCP6041/2/3/4	14 kHz	0.6	3.0	170	1.4 – 5.5
MCP6141/2/3/4	100 kHz	0.6	3.0	170	1.4 – 5.5
MCP6231/2/4	300 kHz	20	5.0	52	1.8 – 5.5
MCP6241/2/4	550 kHz	50	5.0	45	1.8 – 5.5
MCP6001/2/4	1 MHz	140	4.5	28	1.8 – 5.5
MCP6271/2/3/4/5	2 MHz	170	3.0	20	2.0 – 5.5
MCP6281/2/3/4/5	5 MHz	445	3.0	16	2.2 – 5.5
MCP6291/2/3/4/5	10 MHz	1100	3.0	8.7*	2.4 – 5.5
MCP6021/2/3/4	10 MHz	1000	0.5	8.7*	2.5 – 5.5

* Value is typical at 10 kHz

- Select devices available in PDIP, SOIC, MSOP, TSSOP, SOT-23, and SC-70
- Select devices offer a Chip Select pin for additional power savings
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vironment, thereby sidestepping the field-solver approach.

TYING IT ALL TOGETHER

Most engineers do not use a field solver as a stand-alone tool but, rather, as part of a simulation environment. This environment provides various mathematical techniques that accept a combination of ideological inputs from the schematic netlist, as well as some layout or physical modeling from the field-solver module. Ben Mika, design engineer at On Semiconductor, states: "Our designs operate at 3 to 5 GHz; therefore, [you must include] the parasitic contributions of interconnects and long-range couplings between inductive elements, both intentional and parasitic … in the simulations at an early stage … to make any meaningful prediction about the circuit performance." The simulator can have Spice, LNA (linear-network-analysis) harmonic balance, and other simulators. LNA techniques input S-parameters or Spice models from real-world networks to the simulator based on data from VNAs or TDR. A designer may also contribute "fudge" factors based on experience or design safeguards. **Figure 2** shows how a field solver can fit into a signal-integrity or RF-design flow. The user inputs the schematic, and perhaps a mechanical group supplies 3-D CAD models for the field solver. The simulator can teach the user to change the schematic, but two levels of abstraction are available at the first pass. For instance, you could use a fixed inductance to represent a spiral inductor or a slightly more complex lumped-element Spice model that takes into account that the inductance will change with frequency.

Alternatively, you could enter the physical representation of the inductor into the field solver as a 3-D model, or you could get the 3-D CAD data from a mechanical package, such as Solidworks. You can use that representation, along with user-entered data about dielectric constants and conductance, to generate an S-parameter or an LRGC model that represents the inductor better that a fixed-inductance value. After simulating and perhaps changing the schematic or some schematic values, the user can then lay out the IC or board. At this time, the user can feed physical-layout information of metal traces back to the field solver so that it can model the interconnections. Better yet, the field solver can solve for mutual effects between conductors and spiral inductors. The user can then send this information back into the simulator for time- or frequency-domain simulation. This approach yields a design that has a far greater chance of meeting all the design criteria and behaving properly.

The field-solver simulation environment can support two broad categories of design: signal integrity and RF design of an IC, a module, or a board. In the context of providing useful design work, you should view a field-solver program as a component of the total simulation environment.

Several companies make high-end simulation environments for signal integrity. Cadence, with its Spectre simulator, dominates the IC-design market. Mentor offers Eldo for RF design, and Synopsys offers the well-known HSpice environment. Synopsys also offers HSpice-RF, which adds harmonic-balance and frequency-domain analysis to the traditional time-domain Spice tool. Ansoft, with its Nexxim simulator, is also well-known in simulation. The simulator plugs into the company's Designer SI GUI that can then call on Ansoft's well-respected HFSS (high-frequency structure simulator) 3-D field solver or the company's SiWave or Q3D solvers.

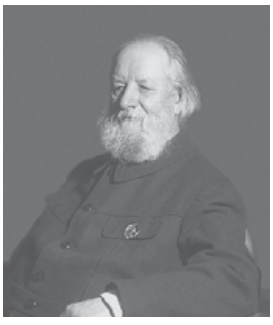
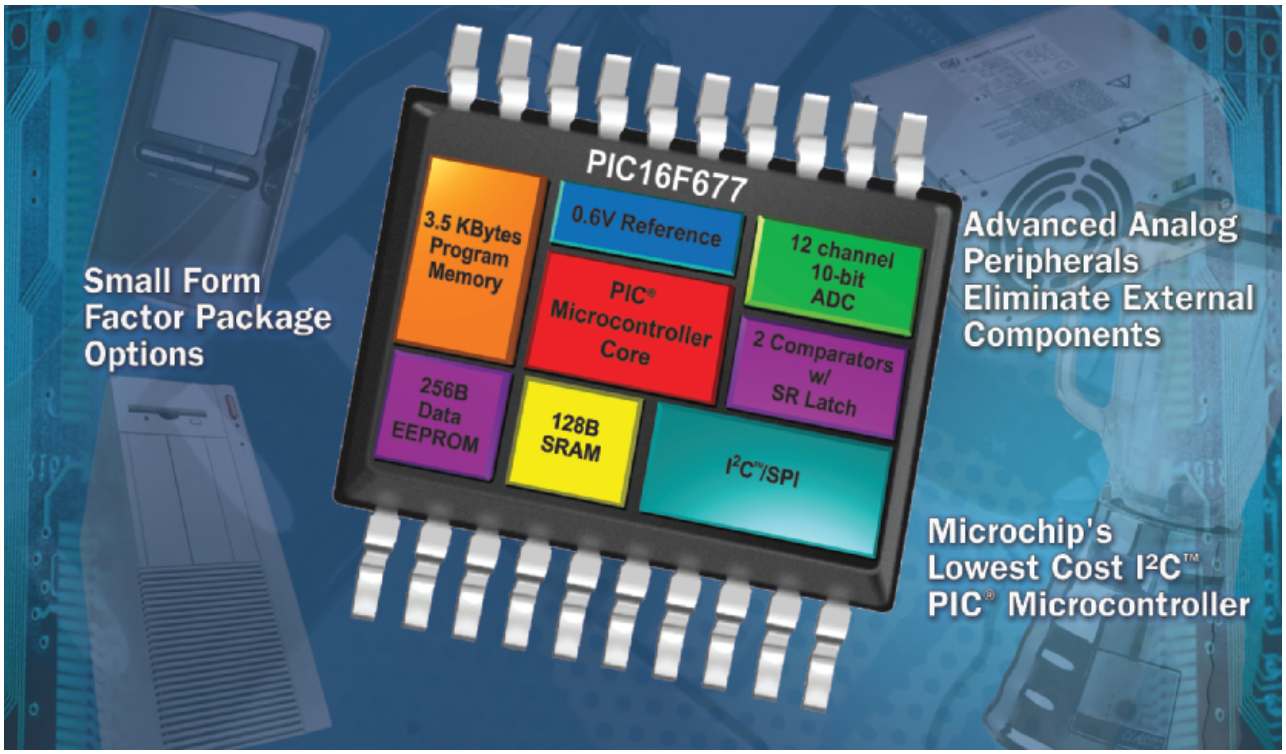


Figure 7 Russian naval officer Alexei Krylov invented the mathematical technique that modern harmonic-balance simulators use.

Perhaps the most sophisticated field solver is the Comsol multiphysics solver. Comsol chose to solve partial differential equations for the problems as a general case, allowing users to employ the company's solver for fluid flow, structural mechanics, heat transfer, and EM. The multiphysics capability enables the solver to solve for the EM fields of materials that are also changing properties or shape due to thermal expansion or magnetic saturation. **Figure 3a** shows the field solution for a power

Simple Control for Complex Applications



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	PIC16F685	4096	256	256	12	2/1	ECCP+	PDIP, SSOP, SOIC, 4mm x 4mm QFN
	PIC16F687	2048	128	256	12	1/1	EUSART, SPI/I²C™	PDIP, SSOP, SOIC, 4mm x 4mm QFN
	PIC16F689	4096	256	256	12	1/1	EUSART, SPI/I²C™	PDIP, SSOP, SOIC, 4mm x 4mm QFN
	PIC16F690	4096	256	256	12	2/1	ECCP+, EUSART, SPI/I²C™	PDIP, SSOP, SOIC, 4mm x 4mm QFN
	PIC16F785	2048	128	256	12	2/1	Op Amps, CCP, Hardware PWM	PDIP, SSOP, SOIC, 4mm x 4mm QFN

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inductor, and **Figure 3b** shows the fields for a spiral inductor. The program can read and operate on Spice files, although the Spice engine has fewer features than those from Cadence, Ansoft, Synoptics, Applied Wave Research, and Agilent.

Coming in from the microwave world, but able to handle signal-integrity issues as well, Agilent offers both the enterprise ADS environment and the desktop Eagleware product that targets individuals and small companies. Applied Wave Research offers Microwave Office and Analog Office, a product that supports signal-integrity and frequency-domain analysis (**Figure 4**). The MathWorks has just announced an RF-design and signal-integrity package for its Matlab environment.

ELIMINATING JUST ONE SPIN OF SILICON FOR AN IC OR ONE REDESIGN OF A COMPLEX BACKPLANE OR DAUGHTERCARD CAN OFFSET THE COST OF ALL THE SOFTWARE AND HARDWARE.

PC-board designers have long grappled with signal-integrity issues. In this area, the well-known brand is Mentor Graphics' Hyperlynx 2.5-D field solver that works intimately with Mentor's PADS brand of schematic and layout tools. It also accepts output from Cadence's Orcad layout tool, which exports to Hyperlynx format (**Figure 5**). Do not confuse the Orcad layout program with the Orcad Editor suite, which uses a stripped-down version of the enterprise-class Allegro board-layout package. When using Orcad Editor, it makes more sense to use Cadence's signal-integrity package, which works seamlessly with Allegro. One notable board-level product that includes signal integrity is Altium's Designer package, which costs less than $5000 for a single license and $5000 more for the schematic-entry and Spice packages. In contrast, the Hyperlynx tool alone costs $5000 to $48,000, depending on fixed- and floating-license requirements as well as functions, such as lossy-transmission-line support. All the "big-iron" environments from Cadence, Ansoft, Synopsys, Agilent, and others have prices starting at approximately $5000 for simple modules, but users can expect to spend $50,000 and up to get a complete simulator with field-solver and layout functions. The desktop-class products such as Microwave Office and Eagleware generally cost $5000 to $25,000 for a usable system. One remarkable exception in the vagaries of pricing is Zeland Software, which provides a full pricing sheet for all the packages and suites that it sells.

Scads of third-party tools exist for high-end design environments, such as those from Cadence. These tools can plug a field solver or other specialized simulator into the design flow. Indeed, Ansoft has taken care to ensure that you can separately plug all of its parts, including the simulator, layout package, and field solvers, into Cadence's and other companies' design flows. IBM even offers the free, "method-of-the-moment," 2-D CZ2D field solver (**Reference 7**). IMST (Informatik und Mikrosystemtechnik) offers its Empire field solver that runs under Windows and Linux. Helic's VeloceRF RFIC-design tool plugs into current tool flows. Sonnet Software offers a 2.5-D field solver that plugs into many design environments, including those of Applied Wave Research. Zeland offers field solvers, Spice tools, transmission-line tools, and filter-design tools, as well as signal-integrity support. The test equipment you need to verify the field solvers costs approximately $2000 on eBay to more than $60,000 for the newest and fastest VNA and TDR models. Microwave and signal-integrity design is not for the faint of heart. Bear in mind, however, that eliminating just one spin of silicon for an IC or one redesign of a complex backplane or daughtercard can offset the cost of all the software and hardware.

When you use field solvers for signal-integrity problems, the stimulation is in the time domain. In this case, a common requirement is measuring an eye diagram (**Figure 6**). In the real world, you obtain this diagram by running a pseudorandom generator into the trace, connector, cable, or system and looking at the receiving end with a scope that can capture and store the repeated traces overlaid on one another. The thickness of the signal

RAQ's

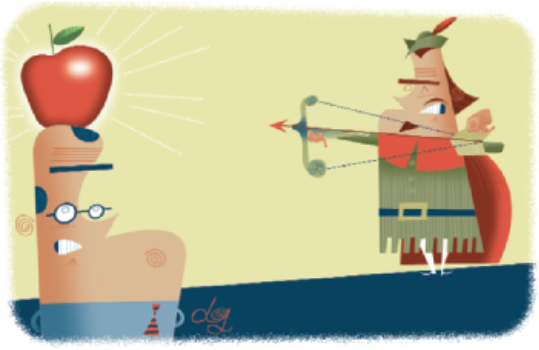
Rarely Asked Questions

Strange but true stories from the call logs of Analog Devices

Contributing Writer James Bryant has been a European Applications Manager with Analog Devices since 1982. He holds a degree in Physics and Philosophy from the University of Leeds. He is also C.Eng., Eur.Eng., MIEE, and an FBIS. In addition to his passion for engineering, James is a radio ham and holds the call sign G4CLF.

Just How Accurate was William Tell, Anyway?

Q. *How accurate is an ADC?*



A. Modern ADCs are extremely precise, but their absolute accuracy does not always match their precision. If young Walter had happened to have a 10 cm apple on his head, William Tell could have afforded less than 5 cm of error. At a range of 50 m (and it was probably no more—in Bürglen today there is no central open space more than 50 m across)[1], this represents an error of one part in 1000, approximately 10-bit accuracy. A 16-bit ADC has a resolution of 1 part in 2^{16} (=1 part in 65536 or 15 parts per million [ppm]), and it is not uncommon for such ADCs to have linearity approaching 1 least significant bit [LSB]. This means that the transfer characteristic deviates from a straight line by less than 1/65536 of full-scale.

For most applications this linearity is far more important than absolute accuracy, but there are cases (ask William) where the absolute accuracy matters.

No presently available 16-bit ADC has an absolute accuracy of 15 ppm relative to full-scale. The best 16-bit ADCs have gain errors of several LSBs. So even with a perfect reference their initial absolute accuracy is, at best, about 14-bits or so. Of course we can calibrate them to well over 16-bits and even provide temperature compensation, but off the shelf they are probably closer to 14-bits.

This does not consider the voltage reference. Because most applications require linearity but not absolute precision, the voltage reference on the chip of many ADCs is about 10-bits accurate, and some are less. This is because a high-precision reference is quite large, would make the converter more expensive, and is not needed by most users.

Separate references are better, but still nowhere near 16-bits. The best available has an initial accuracy of 1 mV in 10 V, about 13-bits. Most high-performance references are of the order of 11- to 12-bit accurate. Even with calibration it is hard to achieve 16-bits, and it is very difficult to maintain it over temperature.

In most ADC applications relative accuracy and linearity are important, but absolute precision is not. Where higher absolute accuracy is necessary it is important to design a system that can be calibrated, and temperature compensated to the level required, and to understand the fundamental limitations of converters and references from any manufacturer. Remember that whatever its resolution the absolute accuracy of an ADC with an internal voltage reference is rarely more than 10-bits before calibration—much the same as old Bill achieved.

Footnote:

1 http://uk.myswitzerland.com/en/swisscams/cam_detail.cfm?webcam_id=1016239307&rkey=2155

To learn more about ADC accuracy, Go to: http://rbi.ims.ca/4946-101

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crossing indicates jitter; the bigger the eye diagram, the better the signal integrity. Simulators working with field solvers can simulate this diagram and give designers an indication of how well the interconnects will perform in real life. You can use this channel modeling to evaluate not only signal integrity in the case of eye diagrams, but also the channel itself on more basic analog-performance criteria. If the time-domain analysis shows no reflections along the entire length of the channel, then you can rest assured that any analog signal will be of higher fidelity than if there were significant reflections.

The field solver can output LRGC models directly to the Spice engine, or the simulator environment can convert S-parameter files from the solver to a time-domain representation with the convolution operation. "Signal integrity is all about the time domain," says Sanjeev Gupta, an application engineer at Agilent. "The models are [in the] frequency domain because, at these frequencies, dispersion and radiation take place,

SIMULATORS WORKING WITH FIELDS SOLVERS CAN ESTABLISH ANOTHER VALUABLE CRITERION: THE AMOUNT OF ENERGY THAT THE BOARD OR THE IC IS RADIATING.

and [you can most easily represent these phenomena] in the frequency domain. People use the frequency domain to describe the channel models, but the system specifications are in [the] time domain, essentially as eye diagrams. So, people need to find out the time-domain performance of these frequency-domain models."

Simulators working with fields solvers can establish another valuable criterion: the amount of energy that the board or the IC is radiating. This information can help predict performance for FCC (Federal Communications Commission) radiation limits and susceptibility under European CE (Conformité Européenne) rules. By having the evaluation occur in software at the beginning of the design, an engineer can predict the performance of the system and prevent a crisis when the product fails FCC certification or, worse yet, does not work at all. "With a lot of our customers, we are embarking on EMC [electromagnetic-compatibility]-radiation analysis, says Mary Tolikas, director of business development for Ansoft. "We model the computer box with ventilation holes and other features and evaluate the radiation."

S-parameters are essential to microwave designers, who are often more comfortable designing and analyzing in the frequency domain. Microwave engineers rarely use a time-domain Spice simulator, preferring LNA or harmonic-balance simulations to solve circuit behavior in the frequency domain. Harmonic-balance and LNA programs focus on the steady-state behavior of electronic systems. By operating in the frequency domain, harmonic-balance techniques can save considerable time over Spice. But, just as Spice is not a panacea for the time domain, LNA and harmonic balance are inadequate and may be unnecessary to design in the frequency domain. "Computer programs are productivity tools, not substitutes for talent or thinking," says James Long, an RF-engineering consultant. "All they do is save design time. Look what was around in 1970 before CAD programs: millimeter microwave, communication theory, ICs, and space flight. If you split the system into blocks, [you'll find] numerous free and low-cost utility programs you can use. Spreadsheet programs have math and graphics abilities. You can write your own utility programs." No responsible engineer sends a circuit to production based only on simulations.

Harmonic-balance techniques solve Kirchoff's voltage laws in the frequency domain. The laws state that, at any point in an electrical circuit where charge density is not changing in time, the sum of currents flowing toward that point is equal to the sum of currents flowing away from that point. Harmonic-balance simulators use a technique that Russian mathematician and naval officer Alexei Krylov invented in the early 20th century

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(**Figure 7**). The Krylov technique solves microwave problems more quickly than time-domain solvers can. The harmonic-balance technique can quickly solve for a microwave signal operating at a single frequency. A Spice time-domain solver breaks the analysis into extremely small time steps and then solves for many of them before the circuit reaches its steady state. Harmonic-balance techniques assume that the system has reached steady state. It can then solve the linear-algebra problem as a sparse-matrix problem. This approach solves for one frequency. Entering a command, such as "order=5," commands the simulator to solve for the fundamental and the first four harmonics of that fundamental. A few harmonics contain almost all of the energy in a microwave system, so the speed and efficiency of the harmonic-balance technique are advantages in solving those kinds of problems. Most microwave and RF simulators also have other modules, or S-parameter simulators, such as LNA, that can operate on the S-parameter data and solve for the performance of high-frequency systems.

"It used to be that you could do pretty good millimeter-wave and RF design just from S-parameters," says Scott Wedge, senior staff engineer at Synopsys. "Empirical-modeling techniques would turn geometries into S-parameter models. For years, we were doing this [step] because EM-solver technology was so slow and expensive. Now, several EM tools are pretty powerful for several types of applications. They've reached the point at which they are overtaking these old modeling approaches. You can throw everything into an EM solver these days. The choice you need to make is whether to do a 2-, a 2.5-, or a 3-D full-wave solution."

Spice can take a high-speed-design problem only so far. After that point, designers need to use advanced simulators with field solvers to properly predict the operation of the circuits. The field solver solves for the performance of one of the most important components in your design—the pc-board or IC layout. It also shows you how to get high-speed signals across connectors and through cables. The old days of prototyping with "dead bug" ICs and leaded components doesn't work for fast circuits. By learning how to use field solvers, you can reduce the time it takes to get to a working design and teach yourself the intuitive aspects of high-speed design. EDN

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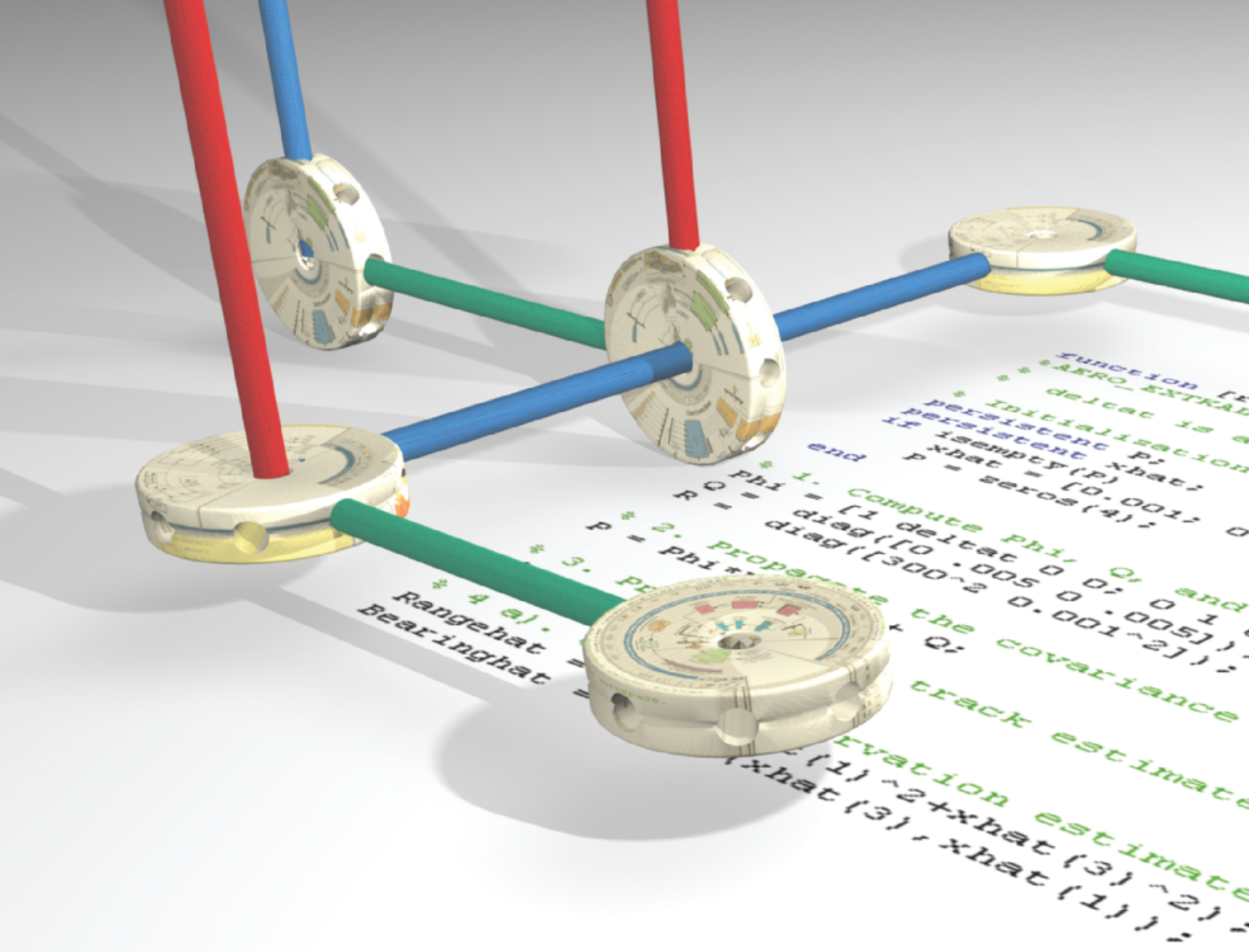

Embedded systems traditionally have limited processing and memory resources to minimize costs, yet consumer expectations are escalating to include more functions along with auxiliary features, such as high-speed communications and interactive multimedia. As the software portions of these embedded projects increase in complexity while schedules shrink, designers are considering graphical-design tools and automatic code generators to augment the limited pool of skilled programmers. With an up-front investment to precisely define the system, design tools can automate some of or the entire software-development task. In many cases, these tools transform embedded-software development from a line-by-line-programming task to a fully automatic process that directly generates operational source code from an abstract model of the system.

Although the thought of replacing a portion of the embedded-software staff with a desktop computer is intriguing, it is not a simple task to sufficiently specify the system for automatic code generators. Current development tools require a significant learning period and possibly a complete change of programming viewpoint before designers are ready to prepare the data necessary for automatic code generation. It may also require a change in mindset among your current software staff to overcome prejudice and accept a different embedded-development technique. Designers have strong opinions when it comes to automatic code generation. Based on early product experience, some developers feel that code generators require substantial overhead and produce inefficient code. Yet, modern tool vendors claim that their code generators produce error-free code that precisely matches the specification and is more compact than handwritten code.

AS EMBEDDED-SYSTEM TEAMS RACE TO BRING NEW PRODUCTS TO MARKET, DESIGNERS ARE EVALUATING MODEL-BASED DEVELOPMENT TOOLS TO DEAL WITH ESCALATING SOFTWARE COMPLEXITY.

MODEL BEHAVIOR: CREATING EMBEDDED-SOFTWARE SHORT CUTS

BY WARREN WEBB • TECHNICAL EDITOR

Automatic code generation is an element or subset of model-based design in which the designer defines the system with a formal graphical representation instead of a traditional written specification. The model must unambiguously define the intended functions and behavior of the proposed system. In general, most system-modeling programs allow the user to construct a system representation by selecting prebuilt blocks from a library and connecting them to form the graphical model. Becoming adept at system modeling requires the same devotion and training period as learning a new programming language.

PRE-PROTOTYPE CODE

One of the main benefits of system modeling is the ability to simulate the operation of the embedded system before committing the design to hardware. A simulator allows you to test and optimize performance to verify that the system meets requirements. A PC-based simulation does not duplicate the deterministic performance of a real-time system yet allows you to test many functions, such as the user interface. Most modeling systems also have built-in error-checking features to automatically check for inconsistencies and ambiguities to eliminate potential mistakes early in the development cycle. Coupling a graphical model with a simulator and code generator can produce operational system software even before the prototype hardware is available. This approach is especially effective in troubleshooting and debugging the first hardware prototypes because it exercises all functional paths (**Reference 1**).

Some modeling systems offer reverse-engineering to automatically synchronize and update the model when you change object code in the lab. This feature connects the design and coding activities and guarantees that the model always reflects the latest product status. Reverse-engineering also implies that you can directly create a model from any embedded source code, but success depends on the way the developer created the code. Most modeling programs also allow the user to extract all system data, in both graphical and textual formats, to create standard or custom system documentation. Like reverse-engineering, automatic documentation ensures that the paperwork tracks the hardware.

The UML (Unified Modeling Language) is one of the popular standards developers use to prepare models for automatic code generation. The industry in 1997 first adopted UML, a

consolidation of as many as 50 modeling approaches developers advanced in the early 1990s. The OMG (Object Management Group) maintains UML, and you can download the latest version of the specification plus tutorials without charge from its Web site at www.uml.org. UML is a nonproprietary graphical technique for capturing the analysis and design of object-oriented software. As with any other object-oriented method, UML is based on classes and objects. A class is a set of objects that have the same data and behavior. Class attributes define the encapsulated data, and class services describe the functions that act on attributes. The latest UML specification defines 13 diagram types to document the software system from the behavior, interaction, and structure points of view.

IBM offers one of the first and most widely used commercial UML modeling tools: Rational Rose. IBM has versions for development of standard business and real-time embedded-software systems. For example, the Rational Rose Technical Developer software is a UML-model compiler that generates complete C, C++, and Java code for Unix, Linux, Microsoft Windows, and RTOS targets. In addition to runtime-model execution, visual-model debugging, and model-based testing, the package includes a porting wizard that provides support for virtually any 8-bit or larger target platform. The software also offers forward- and reverse-engineering support for some of the most common Java constructs. Rational Rose automatically updates configuration management in the background to support remote team development. Prices for IBM's Rational Rose Technical Developer software plus 12 months of support start at $5995.

Specializing in real-time embedded software, the Rhapsody Visual Programming Environment from Telelogic integrates development into a single process in which design, code, and documentation continuously synchronize. You can generate C, C++, or Java directly from a UML model, merge your design with legacy code, or add your own custom code. You can also extract software components from a model and use them in new designs without the need for support from the original developer. **Figure 1** shows a representative user interface for the Rhapsody in C programming environment. The recently introduced Version 7.0 of Rhapsody features an enhanced user interface, reverse-engineering of legacy code, and seamless integration with the open-source Eclipse development platform. Telelogic offers unique software versions depending on the type of code produced and the target operating system. Prices start at slightly more than $1000 for Rhapsody, and typical bundles sell for $10,000 to $20,000.

You can try UML without the expense of an off-the-shelf commercial program using one of several free alternatives. Both IBM and Telelogic offer free, although huge, time-limited trial downloads of their modeling software for buyer evaluation. Another possibility is ArgoUML, a free UML-modeling tool and active open-source-development project. ArgoUML is coded in Java and uses the Java foundation classes, allowing it to run on virtually any platform. Although not yet compatible with UML Version 2.0, ArgoUML supports most class, state-machine, activity, use-case, collaboration, and sequence diagrams. In addition to code-generation features, ArgoUML can reverse-engineer Java code and generate the corresponding UML diagrams. Similarly, the Umbrello UML editor, available with the Linux KDE (K Desktop Environment) desktop, is a Sourceforge open-source project that supports most of the latest UML standard (**Figure 2**). Umbrello delivers code generation for C++, Java, JavaScript, Python, Perl, and several other languages, along with reverse-engineering for C++. Unlike many other open-source projects, the Umbrello developer's Web site provides a complete user handbook that describes UML basics and each diagram type.

Many automatic-code-generation systems are based entirely on the UML

AT A GLANCE

- Embedded-system designers are turning to model-based development to shorten software schedules and simplify functional changes or hardware upgrades.
- Although complex, the Unified Modeling Language provides development teams an open standard to model the architecture of embedded systems.
- With built-in error checking, automatic documentation, and reverse-engineering, modeling software eliminates many common software mistakes.
- System models and simulators allow designers to test system performance and prepare final target code before delivery of prototype hardware.

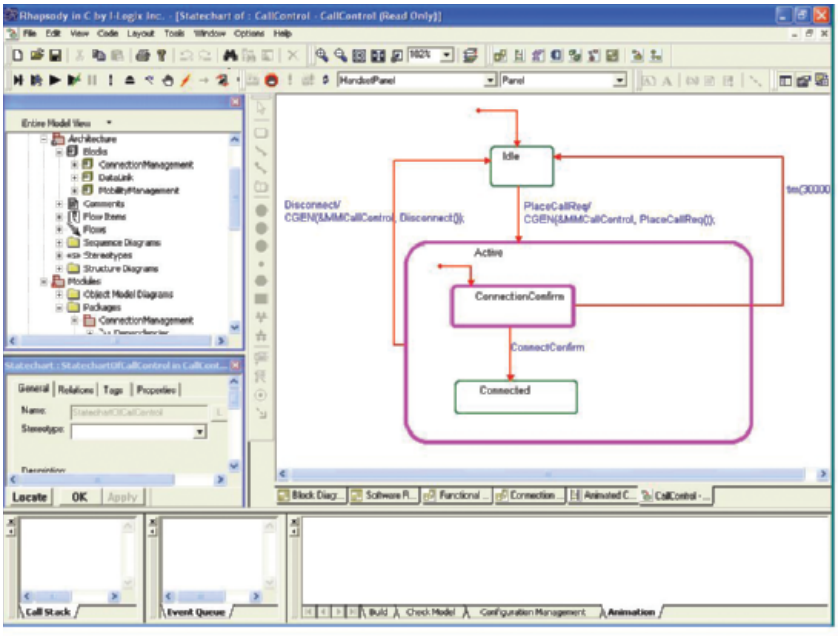

Figure 1 The recently introduced Version 7.0 Rhapsody from Telelogic generates C, C++, or Java code directly from a standard UML model.

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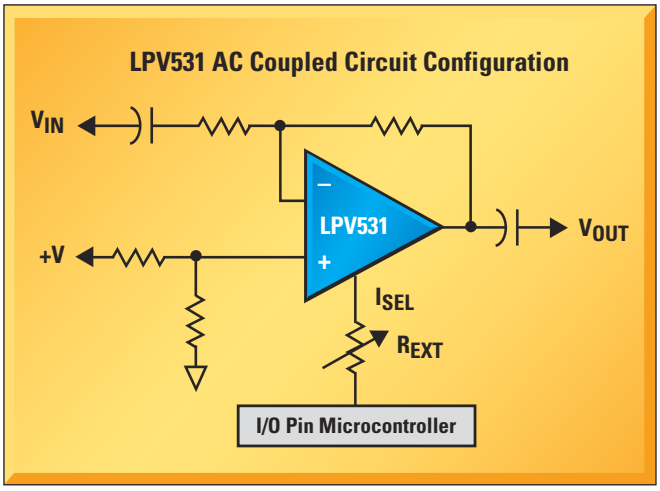

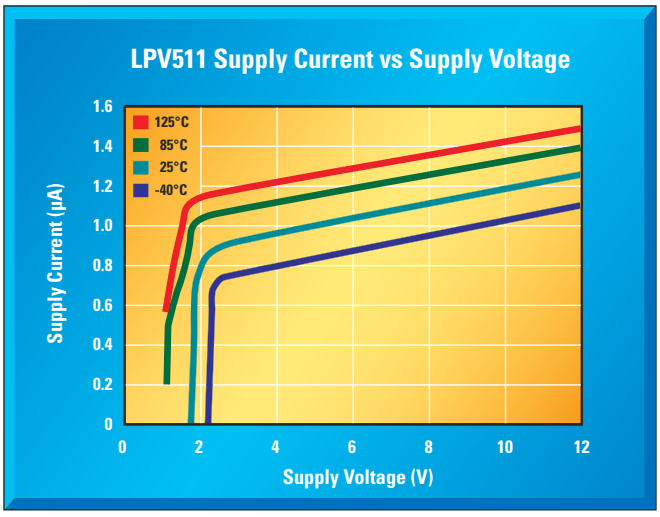

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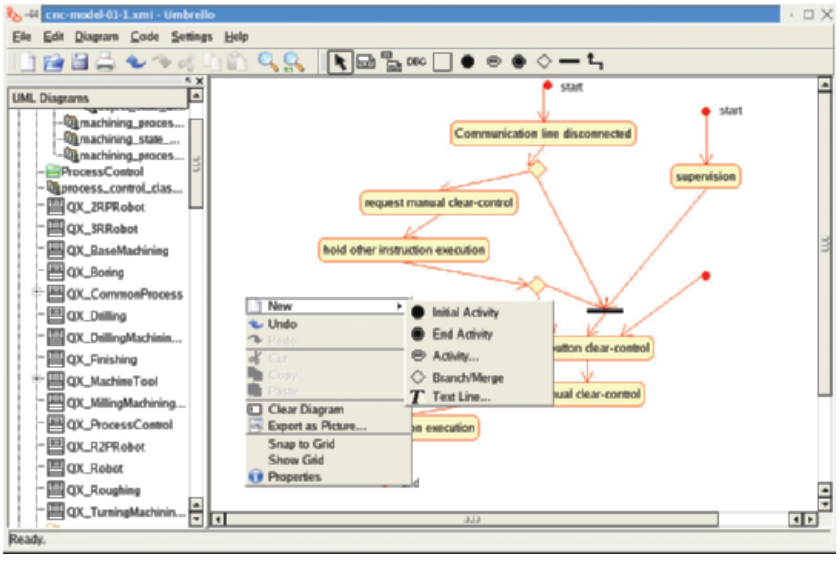

Figure 2 The Umbrello open-source UML editor supports the latest UML standard and generates code for C++, Java, JavaScript, Python, Perl, and several other languages.

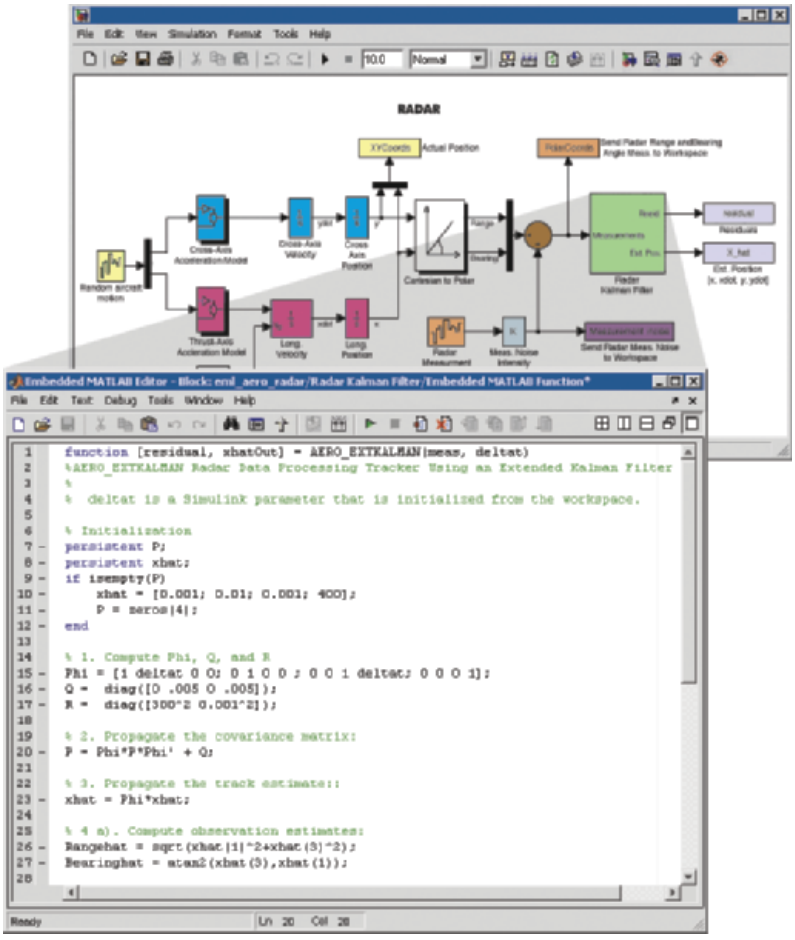

Figure 3 Simulink from The MathWorks allows you to build a model of your system from a library of predefined blocks and evaluate system performance.

standard; however, you can also find several successful software-development tools built on proprietary graphical-modeling systems. For example, The MathWorks offers Simulink, an interactive tool for modeling, simulating, and analyzing dynamic systems. You can build a model of your system from a library of predefined but customizable blocks. You can also divide model elements into subsystems to simplify construction and to enable reuse on multiple projects. The interactive simulator allows you to evaluate system performance and refine your designs. Simulink integrates with The MathWorks' Stateflow for modeling event-driven behavior and Real-Time Workshop Embedded Coder to automatically generate ANSI/ISO-C-compliant code (**Figure 3**). All tools require Matlab, which sells for $1900, and extension tools sell for $2800 for Simulink or Stateflow and $5000 for the Real-Time Workshop Embedded Coder.

TARGET OPTIMIZATION

Gedae, another proprietary, model-based development tool, finds use in intensive signal-processing applications, such as radar, sonar, imaging, and audio. The Gedae tool set includes a workstation-development environment and target-specific runtime kernels for embedded targets, such as PowerPC processors, FPGAs, and DSPs. The Gedae core language specifies the functions of the model without regard to the target or its programming language (**Figure 4**). With built-in or user-supplied implementation parameters, Gedae transforms the model to generate optimized performance for the target. You then export target code to implement the application. Gedae also includes a variety of tools to map applications to multiple processors and visualize the execution activity. Support packages exist for multiple board vendors, and the Gedae BSP (board-support-package) development kit, which allows users to target code to their own custom hardware. Gedae comes in a variety of configurations for algorithm, workstation, and target development with prices starting at $7500.

Recent upgrades to National Instruments' 20-year-old graphical programming language, LabView, provide embedded-software designers with another

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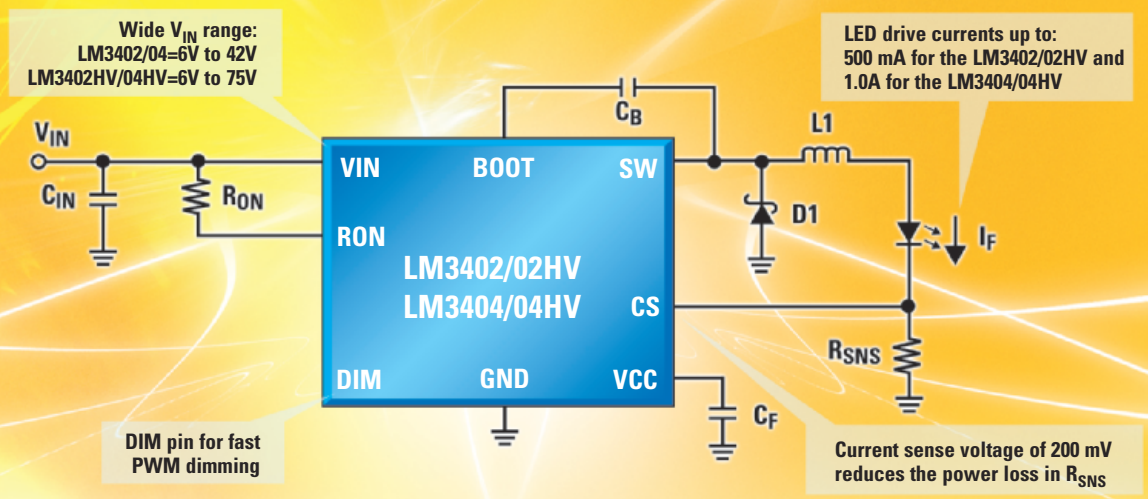

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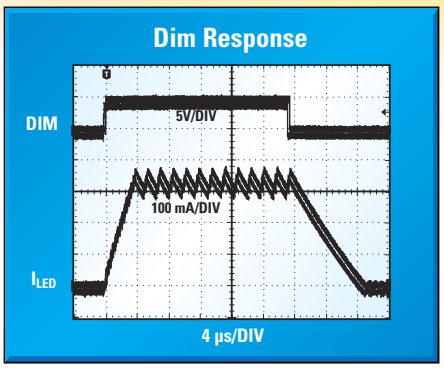

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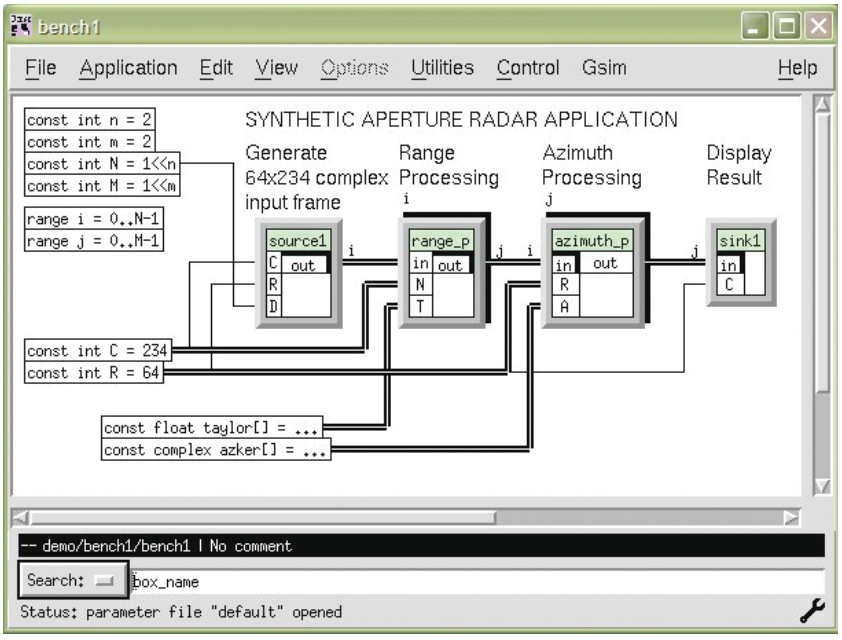

Figure 4 With the Gedae workstation-development environment, users can specify model functions without regard to the target or its programming language.

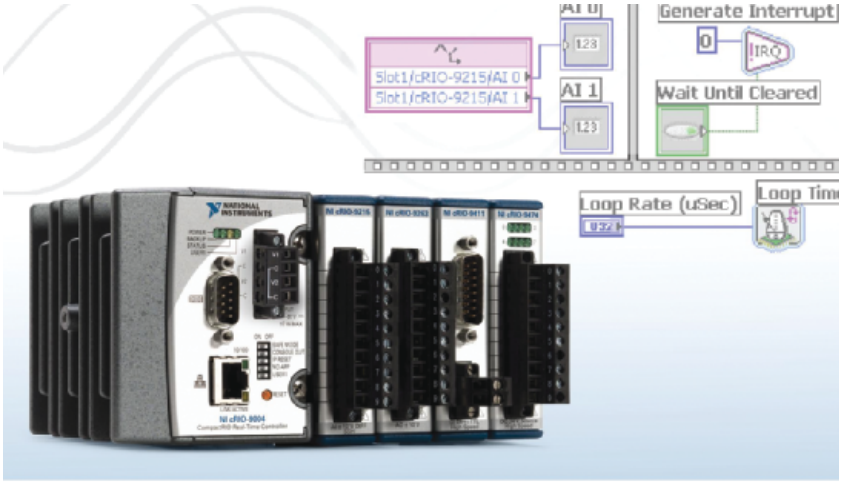

Figure 5 The CompactRIO system from National Instruments defines custom hardware circuitry using a reconfigurable FPGA and LabView graphical-development tools.

avenue for automatic embedded-code generation. In addition to its system-modeling and -simulation features, the latest LabView release supports object-oriented programming with classes; objects; and data-encapsulation, or data-hiding—the mechanism whereby the implementation details of a class are hidden from the user—object-oriented-programming methods. A new embedded-development module provides C-code generation for most real-time operating systems and any target 32-bit processor or DSP. Prices for LabView start at $1199, and the embedded-development module costs $10,995. National Instruments also offers the CompactRIO system, which allows developers to define custom hardware circuitry using a reconfigurable FPGA and LabView graphical-development tools (**Figure 5**). CompactRIO features a real-time embedded processor, a four- or eight-slot chassis containing a user-programmable FPGA, and 15 hot-swappable industrial-I/O modules. The FPGA circuitry at the heart of the CompactRIO system is a parallel-processing computing engine that executes embedded LabView applications at rates as much as 100 times faster than previously possible. Designers program CompactRIO hardware using LabView, the LabView Real-Time Module, and the LabView FPGA Module. Prices for CompactRIO embedded systems start at $2495.

With software the largest embedded-project-budget item, development teams must consider software-automation tools to reduce the programming burden. CMP Media reports that more than half of all embedded-system projects reach completion at least three months behind schedule, and Venture Development Corp estimates that the number of lines of code per embedded project is growing at an average rate of 46% per year. These statistics point to a growing problem that traditional software-development practices fail to address. Although there are many initial hurdles to cross before adopting a model-based design approach, the savings in code generation, documentation, and product updates will eventually pay the transition costs. **EDN**

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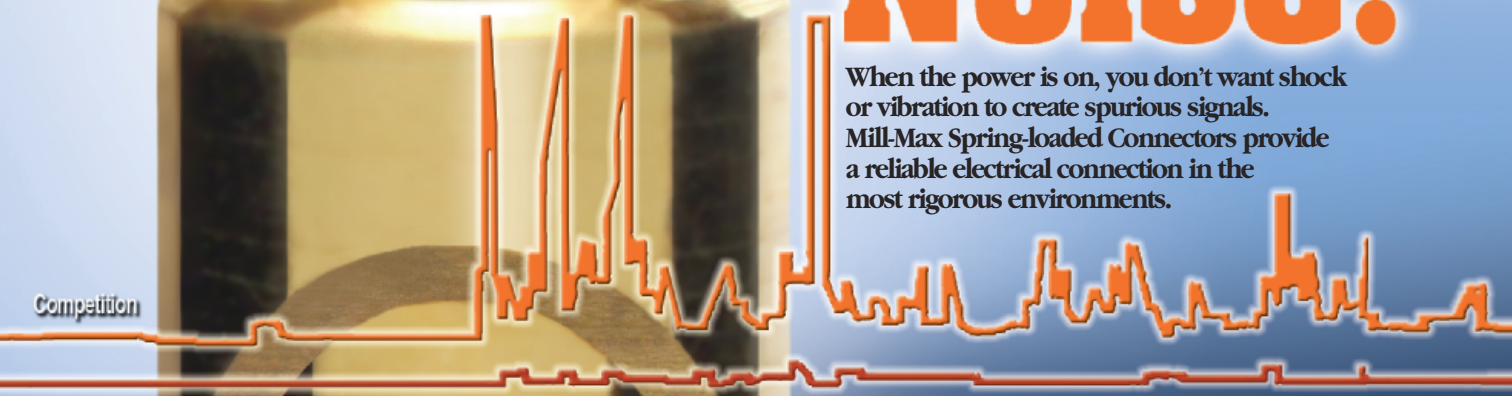

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An effective wireless-sensor network requires the integration of two key components: low-cost, low-power, scalable hardware and manageable software. The industry has shown signs of delivering on the first need with more cost-effective microprocessors and chip sets that allow for lower power communications. A good example is the ZigBee protocol, in which devices can have a duty cycle of less than 1% and an extended battery life of as long as two years using common AA batteries. However, the industry has yet to deliver software that addresses such communications challenges as message routing, node management, and application development.

Before any application development begins, you must configure a sensor network such that nodes can communicate with each other. This step allows for coordination among the sensors as well as some supervisory host communication to the entire network. Unique challenges present themselves when such broad communication is necessary in a power-sensitive environment in which battery life dictates the life of the network. This network communication can be power-intensive, and you must keep it to a minimum; the device needs to spend most of its life in a low-power sleep mode.

When most people imagine a "typical" wireless-sensor network, they imagine many identical intelligent sensors communicating with each other in an ad hoc network (**Figure 1**). In this configuration, each node broadcasts messages to its neighbors on a defined schedule, and messages "hop" from sensor to sensor until they reach their final destination. Because these short-range broadcasts are typically easy on the power budget, this configuration is ideal for optimization of power consumption. Additionally, it requires no central control and therefore is suitable for truly self-sufficient systems. However, this configuration introduces inherent risks concerning the robustness of a network. Because each node will likely be low-cost and effectively disposable, you must plan for a reasonable rate of node failure within the system. In such a configuration, certain nodes can possibly emerge as gateways to large subsections

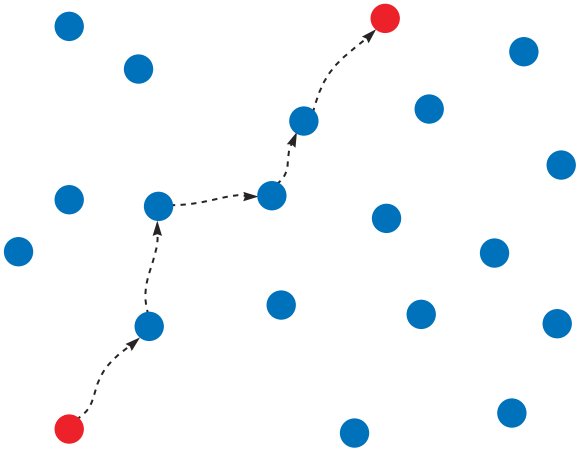

Figure 1 In this example of an ad hoc configuration, each node broadcasts messages to its neighbors on a defined schedule, and messages hop from sensor to sensor until they reach their final destination. These short-range broadcasts are typically power-efficient. However, in ad hoc systems, some nodes can emerge as gateways to large subsections of the network; if these key nodes should fail, these same large subsections of the network will become unreachable.

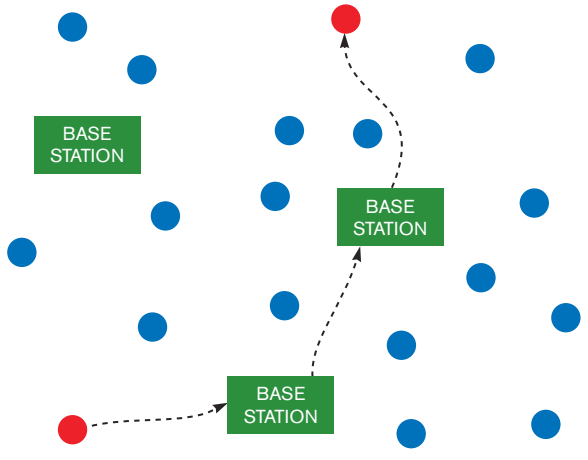

Figure 2 A heterogeneous network requires more power but offers a more maintainable architecture, because each base station represents a single point of failure, and individual sensors can go offline without affecting the rest of the network. The model is similar to a cellular-phone network.

of the network, and if these key nodes should fail, these same large subsections of the network will become unreachable. Although you can reasonably detect and repair these failures, many systems use wireless-sensor networks in remote locations in which simply getting to the sensor is a major expense.

An alternative to the ad hoc network involves overlaying a series of higher power base stations within the network to act as master routing nodes. This configuration, a heterogeneous network, requires more power to run but offers a more maintainable architecture. Each base station represents a single point of failure, and individual sensors can go offline without affecting the rest of the network (**Figure 2**). This model is similar to the one that modern cellular-telephone networks use. Anyone who has experienced a dropped call in the middle of the city knows that the success of any heterogeneous network relies on the strength and placement of the base stations.

When selecting a network configuration, you must take into account the node topology. A static topology is a sensor network in which the nodes are not mobile. An example of this topology is instrumenting a redwood forest for monitoring environmental conditions. The topology naturally lends itself to an ad hoc configuration, because you can strategically place nodes to offer redundant paths to all areas of the network. In addition, although ad hoc networks would likely require a more sophisticated routing strategy, you would need to develop it only once, and it should be applicable throughout the lifetime of the project.

The alternative topology of static is a dynamic topology. In this case, node locations are not fixed, and "nearest neighbors" can change at any point. An example of this approach is a livestock-monitoring system that remotely monitors the health of a herd of cattle. At any point, any one cow could wander past the other, and the network-routing strategy would need to change accordingly. This management requires messaging, and network traffic must thus increase and therefore decrease effective battery life.

A GUI MAKES THE MOVE FROM T&M TO WIRELESS-SENSOR NETWORKS

National Instruments' LabView is a graphical development environment that the measurement industry has used for more than 20 years. It allows engineers and scientists to rapidly and cost-effectively interface with measurement-and-control hardware, analyze data, share results, and distribute systems (Figure A).

Several wireless-sensor vendors, including Crossbow Technology, Accutech, and Accsense (www.xbow.com, www.accu-tech.com, www.accsense.com), are partnering with National Instruments to create LabView drivers to connect to and program their respective wireless-sensor networks. These drivers will allow current LabView users to quickly program and integrate wireless-sensor networks in wired applications with limited or no software learning curve. Figure B shows a sample block diagram with two programs. The bottom program is written with National Instruments' DAQmx software driver to acquire data from a wired data-acquisition device. On the other hand, the top program is reading temperature from a Crossbow wireless-sensor node. Although both are connecting to very distinct hardware technologies, the designers have created the software interface to yield a similar look and feel for the user.

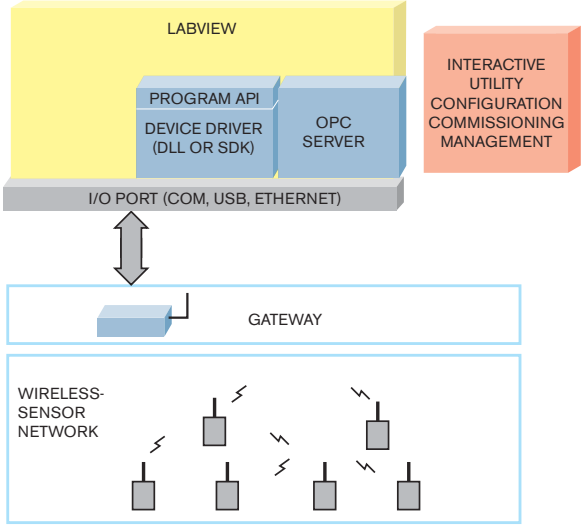

Figure A A GUI such as National Instruments' LabView can provide a unified application-development environment for a wireless-sensor network.

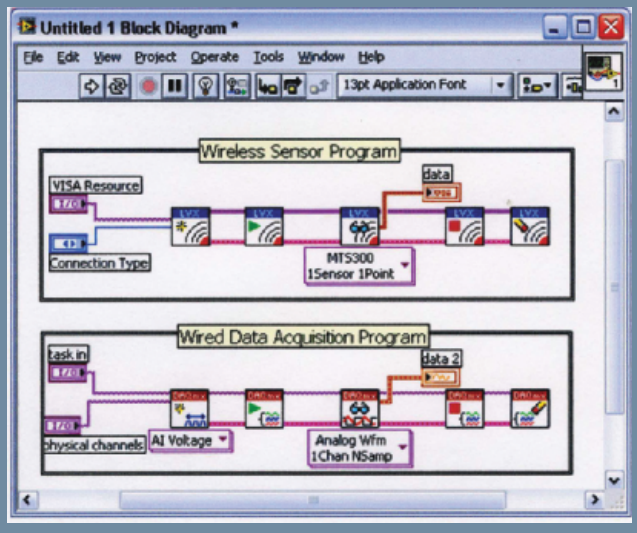

Figure B The bottom program is written with NI's DAQmx software driver to acquire data from a wired data-acquisition device; the top program reads temperature from a Crossbow wireless-sensor node. Although both programs are connecting to distinct hardware technologies, the designers have created the software interface to yield a similar look and feel for the user.

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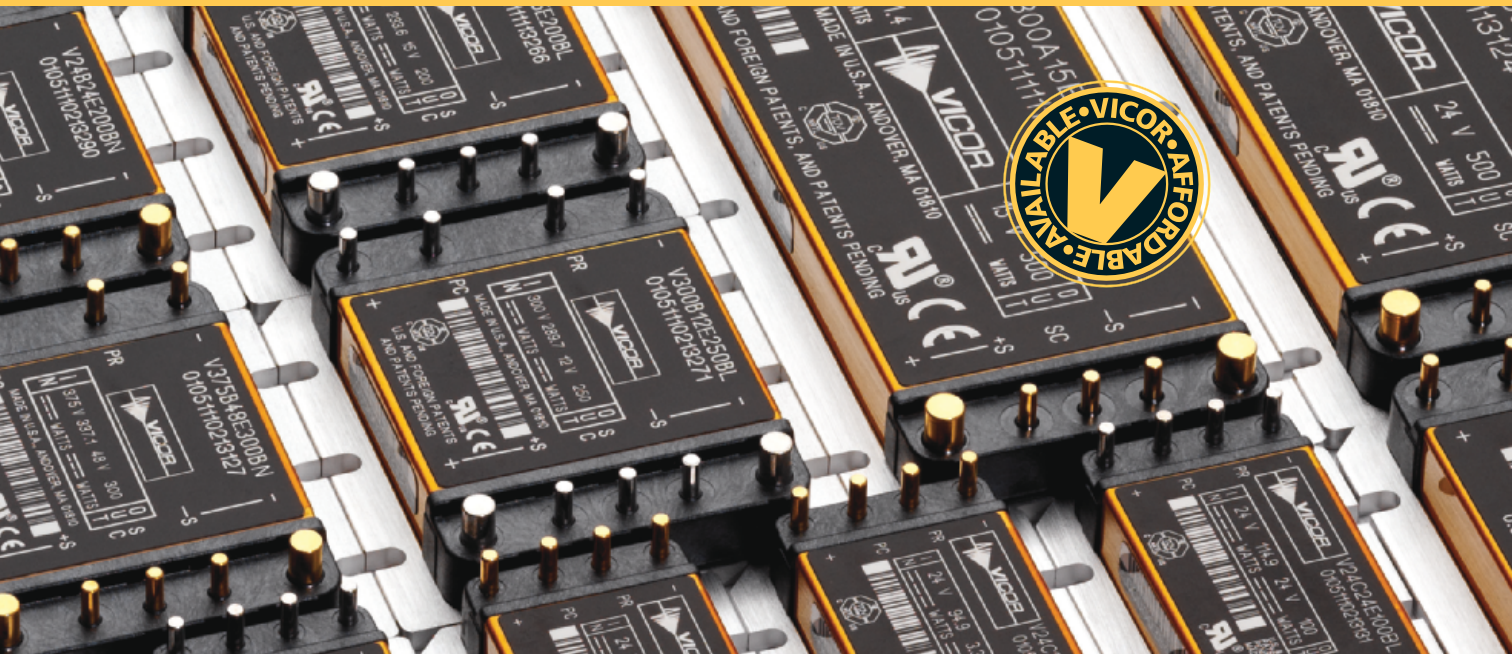

Tracking the location of the sensors as well as the local environmental data further complicates the problem. Keeping with the earlier example in which the network is now tracking the health *and position* of a herd of cattle, you can use a simple survey of node-signal strength to track the location of each cow. This algorithm is relatively simple where you make assumptions about signal degradation over distance and use triangulation to derive approximate position. Because a cow pasture is a relatively open environment in which you can ignore signal reflections, this option is viable. However, examine a use case that uses wireless sensors to track the health and position of firefighters in a burning building. The data requirements are virtually identical, but environmental factors affect the implementation approach. Because signals will likely need to travel through a variety of materials, such as glass, concrete, dry wall, and steel, when transmitted inside a building, you can no longer ignore reflections. Therefore, you can no longer consider the simple signal-strength technique to be reliable. Using this algorithm, any one node could logically be in several different locations, and resolving these conflicts can quickly become too much to manage. In these cases, a GPS (global-positioning system) is a natural fit, because it can provide precise global position. However, a GPS chip set requires a considerable increase to the power budget.

Interference is an additional concern that a wireless-software configuration must address. If wireless sensors truly become ubiquitous, it is reasonable that one network might interfere with another. For example, a home-automation system could reasonably interfere with the firefighter-monitoring system. With this idea in mind, a system must exchange and maintain a unique identifier for each network.

Whatever approach you develop for a network-configuration and -routing strategy, you need to scale their deployments to hundreds, thousands, and even millions of nodes in the future. Moore's Law tells us that commercially available processor speeds double every 18 months. The natural corollary to Moore's Law is that the price of processors of the same frequency decreases over time. Therefore, it becomes more and more economically viable to have an increasing number of intelligent programmable nodes in a wireless-sensor network. Programmers' salaries are not decreasing at a parallel rate, and, therefore, addressing each of these nodes as a separate programmable entity will continue to grow more costly.

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Once you've addressed all of the complexities of the sensor network and determined the routing, communication, and power-management strategies, you still need to complete the application programming of the network. The application software must really exist on three levels: the node, the hub, and the user interface. Software on the node must manage the power consumption and provide enough data processing to minimize data transmissions. In short, the software should ensure that the network sends only the important information and discards the rest. Software on the hub must manage the communication level of the network to maximize battery life. Finally, the user interface must collect all of this information and somehow display it to a user in a way that is intuitive and meaningful (**Figure 3**).

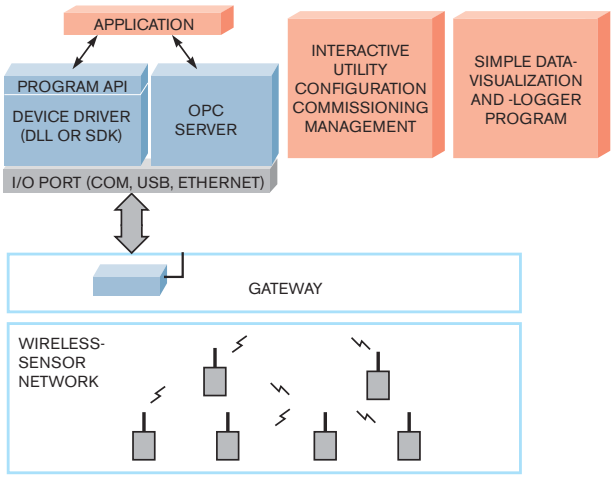

Figure 3 The application software for a wireless-sensor network exists on three levels: the node, the hub, and the user interface. Software on the node must manage the power consumption and provide enough data processing to minimize data transmissions. Thus, it ensures that the system sends only important information and discards the rest. Software on the hub manages the network communication to maximize battery life. The user interface collects and displays system information.

One approach to developing user-interface-level software treats the wireless sensor as an instrument much like an oscilloscope or a digital multimeter. This method allows engineers to abstract the complexity of application development by interacting with the network in a way that is familiar and comfortable. Major players in the wireless-sensor-network industry are addressing this need today by providing driver interfaces to software-development environments such as National Instruments' LabView (see **sidebar** "A GUI makes the move from T&M to wireless-sensor networks").

Node software involves treating the sensor network as a distributed computing cluster. When programming such systems, you develop a single application and execute it on all nodes simultaneously. You give each node some unique identifier, and the software relies on this identifier for its processing algorithm. The advantage of this approach is that, through thoughtful programming, you can write a single application that executes differently on each node, effectively giving the same flexibility of programming each node individually. This approach does, however, require a programmer to understand and apply new programming techniques and refactor or rewrite any existing applications. EDN

AUTHOR'S BIOGRAPHY

PJ Tanzillo has worked at National Instruments for three years, where he is LabView embedded-product manager. He graduated from Ohio State University (Columbus) with a bachelor's degree in electrical and computer engineering. His interests include independent music, art, and films; biking; vegetarian cooking; and politics.

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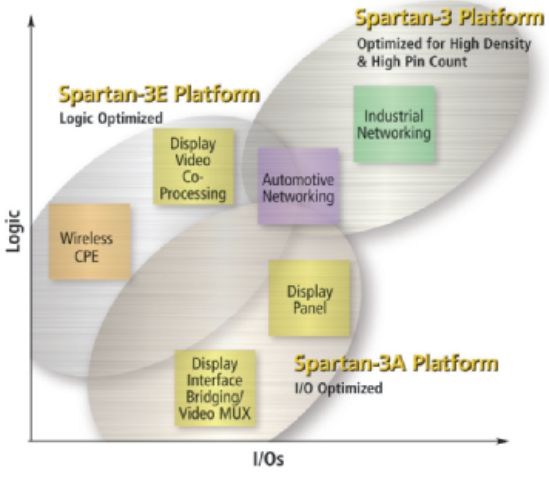

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BRIEF

Detection of RS-485 signal loss

By Kevin Gingerich • *High-Performance Linear/Interface*

Introduction

Fault isolation and safety shutdown protocols are critical in many industrial, telecommunication, automotive, and data processing systems. While built-in test routines can provide fault isolation when the system is offline, real-time fault detection requires continuous monitoring of signals. These systems often use RS-485 to share data between sensors, actuators, single-board computers, and communication processors.

RS-485 signals are differential, using two signal wires to transmit data, and detection of valid signal levels requires a differential window comparator. Designing this circuit function is complicated by the wide common-mode range of RS-485 signals and, in many cases, the availability of only positive supply rails.

This article shows how a differential window comparator can be constructed with the passive-failsafe feature* of two SN65HVD3088E RS-485 transceivers and an AND gate. It also provides theory of operation, the basic circuit schematic, test results, and other design considerations.

Theory of operation

The differential input threshold is the voltage between the non-inverting and inverting RS-485 signals above which the bus state is high and below which the bus state is low. The differential input voltage threshold of standard receivers is between –200 mV and 200 mV. The differential input voltage

*See Reference 1 for more on this feature.

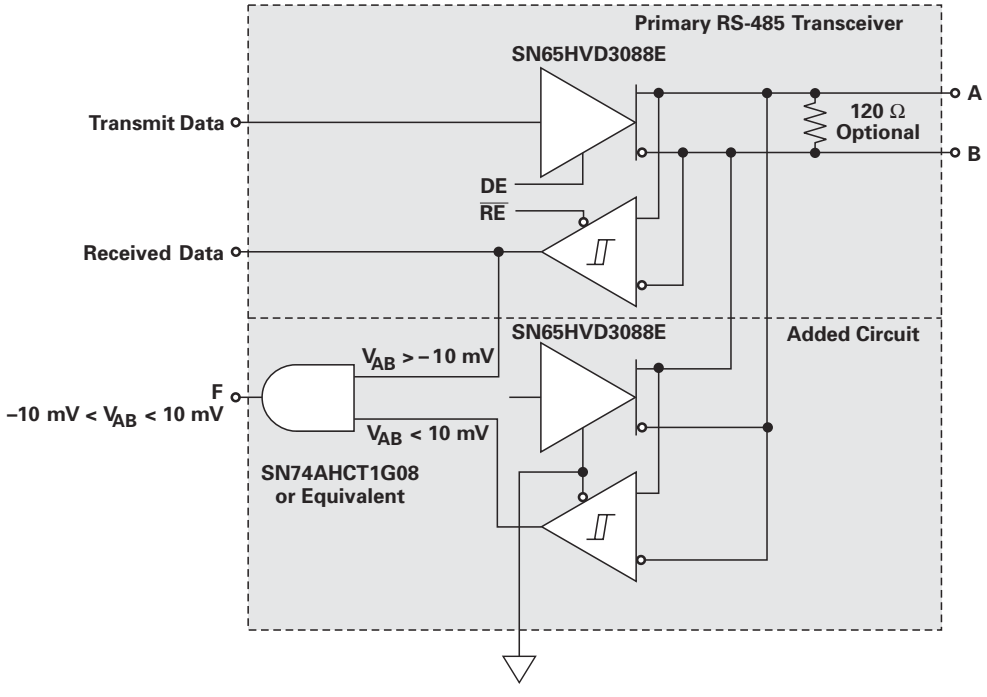

Figure 1. RS-485 transceiver with loss-of-signal indicator

threshold of the SN65HVD3088E is between –200 mV and –10 mV. This gives a known (high-level) receiver output state with zero volts (no input signal) and is called passive failsafe. It does not distinguish between a valid high input and no signal.

A single SN65HVD3088E can determine if the differential input voltage is less than –200 mV or above –10 mV. Reversing the input polarity of a second SN65HVD3088E can determine if the differential input voltage is below 10 mV or above 200 mV and is the basis for constructing the differential window comparator shown in Figure 1.

The upper-receiver output in Figure 1 is true (high) if the differential input voltage, V_{AB}, is greater than –10 mV. Since the inputs of the lower receiver are reversed, the output is true (high) if $-V_{AB} > -10$ mV or, dividing both sides of the inequality by negative one, $V_{AB} < 10$ mV. If both receiver outputs are true, then the differential bus voltage is between –10 mV and 10 mV and is not a valid input. This fault is indicated by the AND gate F output using inputs of the two receiver outputs.

Test results

Figures 2 and 3 show the F and V_{AB} low-to-no and high-to-no signal transitions and the desired fault indication.

Other design considerations

While this example circuit uses the SN65HVD3088E, any RS-485 receiver with the passive failsafe feature can be used (Texas Instruments offers over 30 such products). A similar approach can be applied to unidirectional (simplex) connections. The parallel connection of the two transceivers will halve the unit loading and double the stray capacitance presented to the bus. This may limit the number and spacing of devices on a bus segment (see References 2 and 3).

If the system timing budget allows, filtering of F may prevent false fault indications from differential noise or from very slowly changing input signals. Filtering can be done by adding gating or by choosing a very slow AND gate.

Conclusion

A differential window comparator can be constructed by adding a passive-failsafe RS-485 receiver and one AND gate to another passive-failsafe receiver. The circuit then provides a loss-of-signal indication from an RS-485 data bus. This fault flag can then be used for system fault isolation or safety shutdown protocols.

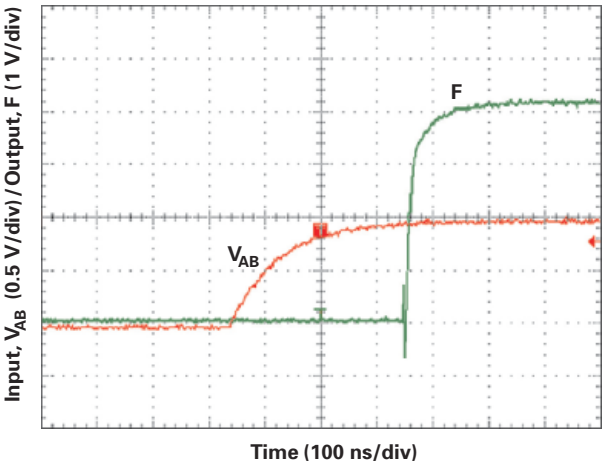

Figure 2. Loss of valid low-level signal

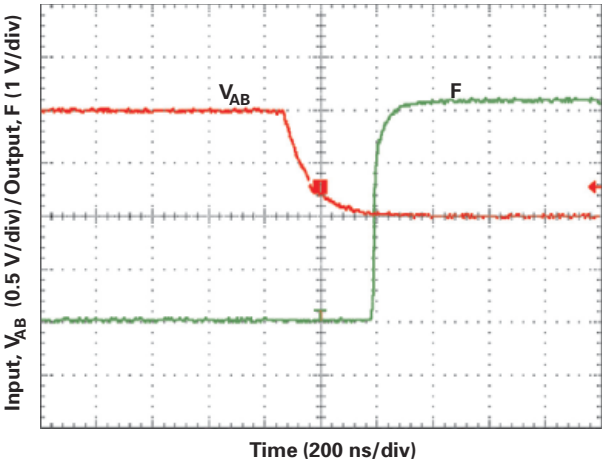

Figure 3. Loss of valid high-level signal

References:

1. Failsafe in RS-485 data buses (slyt080)
2. The RS-485 unit load and maximum number of bus connections (slyt086)
3. Device spacing on RS-485 buses (slyt241)

BY ANN DE VRIES AND YANJUN MA • IMPINJ

A logical approach to NVM integration in SOC design

SOC DESIGNERS HAVE SEVERAL OPTIONS FOR INTEGRATING NVM (NONVOLATILE MEMORY) INTO THEIR DESIGNS, SO IT'S WISE TO WEIGH THE AVAILABILITY AND NUMEROUS TRADE-OFFS BEFORE JUMPING HEADFIRST INTO INTEGRATING NVM INTO YOUR SOC.

Increasingly, ICs require embedded NVM (nonvolatile memory). The popularity of consumer appliances such as MP3 players—with their associated need for digital-rights management—and security considerations, for example, drive this trend. At the same time, recent technological advancements provide designers with many options for integrating on-chip NVM. Understanding the trade-offs among the various technologies equips designers with the knowledge necessary to create the best design in the most cost-effective manner.

Generally, when SOC (system-on-chip) designs require a small amount of NVM, designers might select mask-programmable ROM, battery-backed SRAM, or OTP (one-time-programmable) fuses. For certain design trades, EEPROM and flash memory make sense. Now, logic-CMOS NVM, also known as logic NVM, is also an option. What are the advantages or disadvantages of each choice? How does a choice affect system performance, chip cost, and testability? To better understand which memory best suits your design, it is wise to explore the availability and trade-offs of the various NVM types for fully integrated SOCs. (For more detail on the bit-cell differences among the various NVM technologies, see **sidebar** "NVM-technology overview.")

A hypothetical RF-receiver system serves as a vehicle for comparing the various memory options (**Figure 1**). A brief orientation reveals several strategic opportunities for embedded NVM. At the front end, an analog signal enters a low-noise amplifier and then proceeds through a set of mixers, filters, and ADCs. In the digital path, the design application

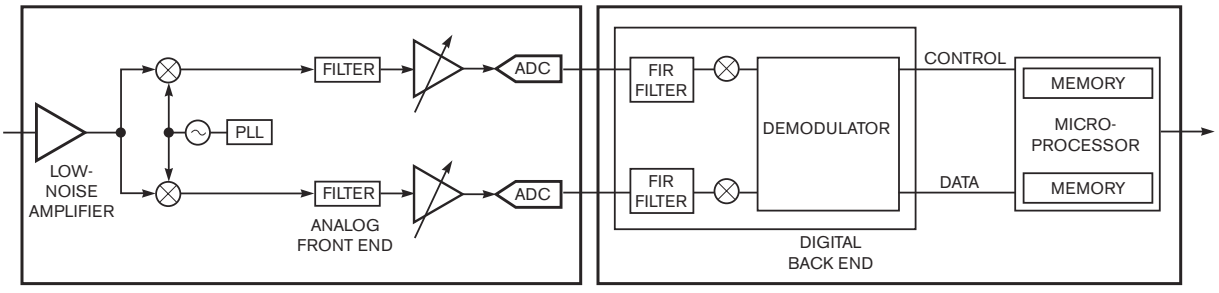

Figure 1 In a hypothetical RF-receiver system, an analog signal enters a low-noise amplifier and then proceeds through a set of mixers, filters, and ADCs.

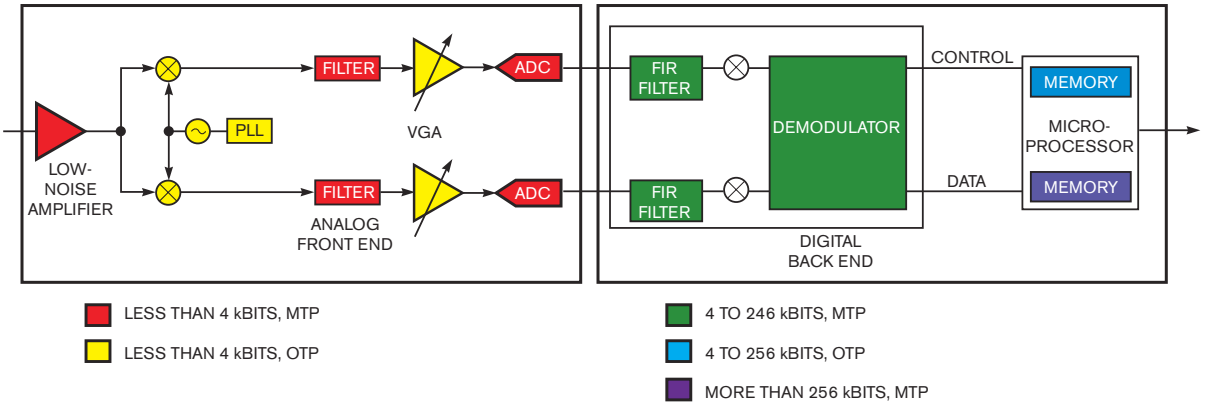

Figure 2 In a mixed-signal system, the front end tends to require more OTP NVM, and the back end requires more MTP NVM.

might suggest additional signal processing, including filtering, mixing, and demodulation, before the data ends up in the microprocessor. In the example, one path provides control, and the other path provides data. The microprocessor manipulates the data according to the application and delivers the information out the back end. So, what opportunities does NVM offer in each stage for enabling the system, improving performance, or simplifying design?

Opportunities exist throughout the design. For example, in the analog front end, small amounts of NVM ensure design accuracy in multiple places: gain adjustment for the low-noise amplifier, trim matching for the signal mixer, filter adjustments for the phase-lock loop, analog-filter coefficients, gain and phase adjustment, and manufacturing trim for the ADC. Process variations invariably alter the characteristics of analog components. The ability to change parameters through NVM storage allows designers to ensure that their circuits operate correctly. Furthermore, temperature changes affect analog-circuit operation. For circuitry operating under conditions of wide temperature swings, the addition of MTP (multiple-times-programmable) NVM or a parameter look-up table based in OTP arms designers with the ability to maintain accuracy of their design in the field.

The larger bus widths associated with a digital back end typically require larger amounts of NVM. The DSP block might require filter-coefficient and demodulation-parameter storage. Once the data enters the microprocessor block, the application might call for decrypting information using frequently changing keys, performing frame synchronization, or storing small code updates. Each of these data requirements varies in when and how often they update, their size requirements, and why the updates occur. **Table 1** provides a summary of the hypothetical system-parameter-storage requirements.

If designers split their memory requirements into three cate-

NVM-TECHNOLOGY OVERVIEW

Today, most embedded NVMs (nonvolatile memories) store information by changing the conductance of the read path in a bit cell. Memory designers use two principal methods to modify read-path resistance: a polyfuse/oxide-antifuse element or modification of the threshold of a MOSFET through charge storage.

Designers typically measure process complexity by assessing how many extra mask steps over logic CMOS they will need to implement the embedded NVM. (Any additional masking layers affect all transistors in the circuit, reducing yield due to the added defects the extra processing steps induce.) Designers must choose among NVMs requiring no added masks, such as logic-CMOS NVM, including polyfuse; two to four additional masks, such as SONOS (silicon-oxide-nitride-oxide silicon); and six to10 additional masks, such as embedded flash. Embedded flash usually requires a second and sometimes a third polysilicon layer. Figure A provides an example of a generic NVM cell.

For a silicided polyelectrical fuse, the storage device is a polyresistor (Figure B). When designers program the device, a current of approximately 10 mA that passes through the "stress/bit" node causes self-heating and electromigration of the silicide and increases the resistance of a narrow section of polyfuse on the field oxide. To read the bit value, external circuitry enables the MOSFET using the "select" node, and then a sense amplifier connected to the "sense" node detects the state. Increased resistance in the read path indicates a change of storage state. But polyfuse circuitry has limitations, including OTP (one-time-programmability) limitations, relatively large cells due to the large programming current, and some reliability concerns over fuse regrowth.

For an electrical antifuse, the storage device is an ox-

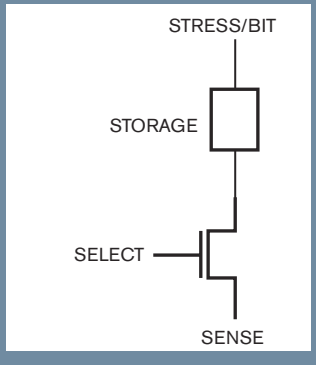

Figure A A generic NVM cell stores information by changing the conductance of a read path in a bit cell.

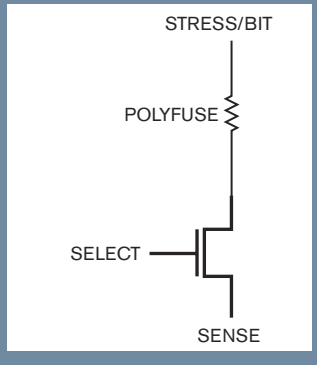

Figure B For a silicided polyelectrical fuse, the storage device is a polyresistor.

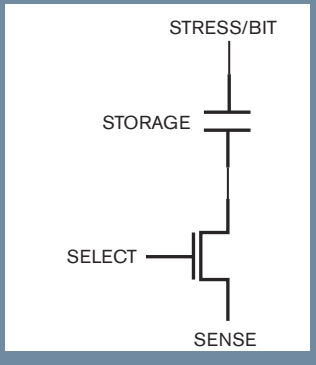

Figure C The storage device for an electrical antifuse is an oxide capacitor.

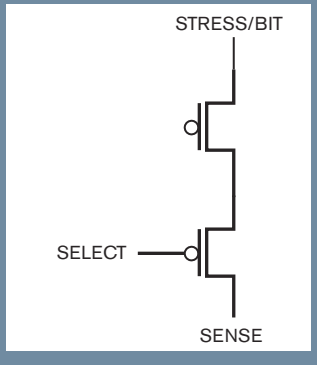

Figure D Most EEPROM and flash products use floating-gate technology.

gories of less than 4 kbits, as much as 256 kbits, and more than 256 kbits, they can go ahead and partition the system accordingly. But they may further subdivide the memory choices into those programmed during manufacturing and those requiring updates over the life of the chip. Designers may divide this mixed-signal system into two chips (**Figure 2**). The front end tends to require less NVM and more OTP NVM. The digital back end, with the associated wider data buses, requires greater amounts of mostly MTP NVM. If an application needs access to more NVM—for example, for large code or data updates—designers may want to provide an interface to external NVM.

If designers must increase system integration, lower cost, and maintain scalability to smaller processes, what options are available? To answer that question, first examine an overview of embeddable NVM characteristics across process types (**Table 2**). (This comparison includes neither ferroelectric RAM nor magnetic RAM.)

Designers can then take a couple of approaches. One method continues the two-chip approach in which designers optimize the design of each piece. Designers may want to use fuse or antifuse OTP NVM for the small amounts of memory in the analog front end. In this case, designers achieve higher program speed than they would using logic OTP CMOS at the expense of higher power consumption. If the design is destined for high production volume, higher program speeds might be an important cost consideration. However, if the design requires field testing and programmability, the only choice is logic OTP CMOS; fuse or antifuse designs require factory programming. Package characteristics can also affect precision analog parts. Postpackage programming might be desirable over wafer sorting, again indicating logic CMOS as the only choice. In either case, manufacturers develop the chips in leading-edge processes, and they require no extra mask charges, which lowers overall cost by yield and increas-

ide capacitor (Figure C). When designers program the device, applying a large voltage at the stress/bit node ruptures the oxide. To read, external circuitry enables the MOSFET using the select node, and then a sense amplifier connected to the sense node detects the state. Reduced resistance in the read path indicates a change of the storage state. The limitations of oxide-antifuse circuitry include OTP problems, some reliability concerns about oxide breakdown, and scalability concerns for advanced processes. (Oxide breakdown is not well-defined for ultrathin oxides.)

Most EEPROM and flash products use floating-gate technology. Figure D shows a floating-gate PFET. The select transistor can be either an NFET or a PFET. The floating FET comes out of fabrication uncharged or may be erased with ultraviolet light, leaving the gate in the off position. Charge injected onto the floating gate from the stress/bit node using hot carrier injection turns on the floating-gate FET. To read, external circuitry enables the MOSFET (select node), and then a sense amplifier connected to the sense node detects the state through the presence or absence of current flow.

For MTP (multiple-times-programmable) logic-CMOS floating-gate technology, a group of floating-gate FETs stores the charge (Figure E). Designers can implement the cell using a standard CMOS process without extra masks or process steps. During programming, pulling the N well of the tunnel PFET to high voltage while keeping the control gate at ground causes FN (Fowler-Nordheim) tunneling, erasing the floating-gate charge. Pulling the control gate to a high voltage while keeping the rest of the nodes at ground uses FN tunneling in the reverse direction to add charge to the gate. Hot carrier injection from the stress node can also program a cell. To read, external circuitry enables the read MOSFET using the select node and determines the current flow through a sense amplifier connected to the sense node.

Charge stored on a floating-gate FET with double polyfuse is the storage mechanism for embedded EEPROM or flash (Figure F). To program, pulling the stress/bit node to a high voltage while keeping the select at ground or at a negative voltage creates FN tunneling, which erases the floating-gate charge. Pulling select to a high voltage while keeping the rest of the nodes at ground uses FN tunneling in the reverse direction to add charge to the floating gate. Hot carrier injection from the stress/bit node can also program the cell. To read, external circuitry uses the select node to enable the cell and determines current flow through a sense amplifier connected to the sense node.

SONOS embedded flash memory works in the same way as the floating-gate flash but replaces the floating gate with a layer of nitride as a charge-trapping medium. SONOS is generally thinner than floating-gate NVM, enabling programming and erasing at lower voltages. The thinner oxide simplifies the process steps to only two to three extra layers from the CMOS baseline process rather than the six to 10 layers for floating-gate NVMs.

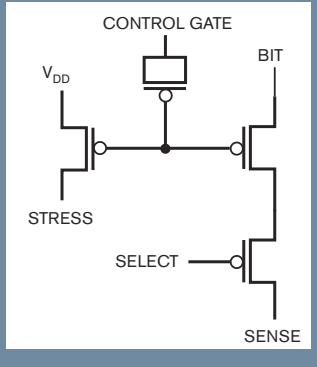

Figure E For MTP logic-CMOS floating-gate technology, a group of floating-gate FETs stores the charge.

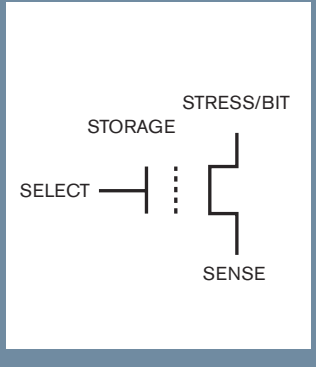

Figure F Charge stored on a floating-gate FET with double polysilicon is the storage mechanism for embedded EEPROM or flash.

es reliability. (Any additional masking layers affect all transistors in the circuit, because the extra processing steps introduce defects, resulting in lower yield and reduced reliability.)

For the digital back end, designers usually go with embedded EEPROM or flash because that course is a straightforward transition from external memory. Embedded EEPROM and flash come with the advantages that both control and data interfaces are already in place. Assuming that designers have a similar architecture for the embedded version, many choices exist. Bringing data storage on-chip also reduces the amount of I/O circuitry. It also allows designers to reduce system bill-of-materials cost by removing external components, lowers board costs because there are fewer lines to route, achieves fast read, and lowers power at the expense of extra process steps. However, if your company determines that six to 10 extra process steps to bring EEPROM and flash on-chip will too greatly impact the bottom line, then it is back to the drawing board. A quest for reduced power consumption and less of a processing hit might compel designers to use SONOS (silicon-oxide-nitride-oxide-silicon) flash, which requires only about three extra masks.

A second approach is for designers to integrate the memory in a single mixed-signal chip. For the OTP NVM, either

TABLE 1 SYSTEM-PARAMETER STORAGE

Parameter	Size	Programmed	Updated	Why
Low-noise-amplifier gain adjustment	Bits to bytes	At manufacture, in field	Temperature dependent	Process variations, compensation
Mixer trim matching	Bits to bytes	At manufacture	No	Process variations
PLL coefficients	Bits to bytes	At manufacture	No	Process variations
Analog filter	Bits to bytes	At manufacture, in field	Temperature dependent	Process variations, compensation
VGA gain/phase matching	Bits to bytes	At manufacture	No	Process variations
ADC trim	Bits to bytes	At manufacture	Temperature dependent	Process variations, compensation
DSP-filter coefficients	Less than 1 kbit	At manufacture, in field	Infrequent	Enable different modes
Demodulation parameters	Less than 1 kbit	At manufacture, in field	Infrequent	Change in modulation scheme
Decryption keys	Multiple bytes	In field	Frequent	Security
Frame synchronization	Multiple bytes	In field	Infrequent	Updates
Boot ROM	10s of kilobits	At manufacture	No	NA
Code updates	100s of kilobits	In field	As needed	Bug fixes, testability, function changes

TABLE 2 EMBEDDED-NONVOLATILE-MEMORY COMPARISON

	MTP			OTP	
	EEPROM/flash	SONOS flash	Logic NVM	Fuse/antifuse	Logic NVM
Cell area	Small	Small	Medium	Medium/small	Small
Process	Two- to three-generation lag	Two- to three-generation lag	Leading	Leading	Leading
Extra masks	Six to 10	Three	None	None	None
Scalability	Difficult for EEPROM/flash scales	Yes	Yes	Yes	Yes
Program mechanism	Tunneling/hot carrier injection	Tunneling/hot carrier injection	Tunneling/hot carrier injection	Electromigration/ permanently ruptured connection	Hot carrier injection
Storage medium	Floating gate	Nitride film	Floating gate	Broken polyfuse/ oxide	Floating gate
Program speed	Milliseconds/ microseconds	Milliseconds	Milliseconds	Milliseconds/ microseconds	Milliseconds
Program power consumption	Medium	Low/medium	Low	High/medium	Medium
Erase mechanism	Tunneling	Tunneling	Tunneling	NA	NA
Erase scheme	Byte/page	Sector/chip	Page/none	NA	NA
Erase speed	Milliseconds/page	Milliseconds/page	Milliseconds/page	NA	NA
Read speed	Nanoseconds	Nanoseconds	Nanoseconds	Nanoseconds to microseconds	Nanoseconds
Field programmable	Yes	Yes	Yes	No	Yes

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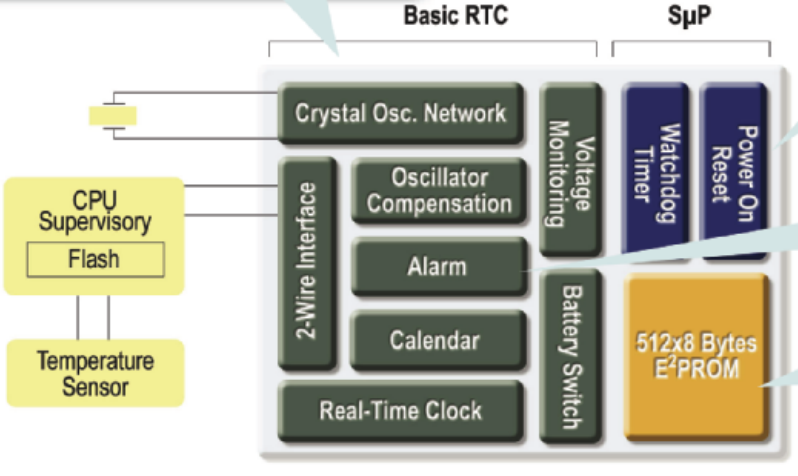

Integrated Power On Reset and Watchdog Timer eliminates external devices.

Two non-volatile alarms can be set to the second, minute, hour, day of the week, day or month.

Integrated 4k Bytes of E²PROM memory reliable for >2,000,000 write cycles eliminates external device.

800nA General Purpose Real-Time Clock Selector Table

	Int. E²PROM (Bytes)	Alarm	CPU Sup.Fx's POR	CPU Sup.Fx's Wdg Timer	IRQ	FOUT	VTRIP for Rest/Bat Switch	Package
ISL12026	512 X 8	2	N	N	$\overline{IRQ}$/FOUT		5 Sel. (2.63V to 4.64V)	8-Ld SO/TSSOP
ISL12027	512 X 8	2	Y	Y	$\overline{RESET}$		5 Sel. (2.63V to 4.64V)	8-Ld SO/TSSOP
ISL12028	512 X 8	2	Y	Y	$\overline{IRQ}$/FOUT		5 Sel. (2.63V to 4.64V)	14-Ld SO/TSSOP
ISL12029	512 X 8	2	Y	Y	$\overline{IRQ}$/FOUT		5 Sel. (2.63V to 4.64V)	14-Ld SO/TSSOP

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TABLE 3 DESIGN TRADE-OFFS

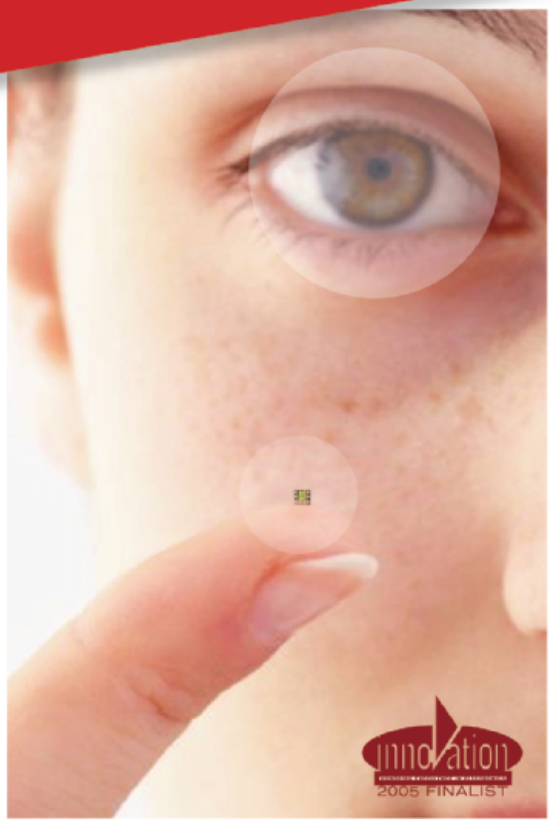
NVM type	Capacity	Pros	Cons
EEPROM/ flash MTP	Megabits	Small cell area, fast reads, large memory	Higher power, greater cost, lower yield, two- to three-generation process lag
SONOS flash MTP	Megabits	Small cell area, fast reads, large memory, scalable	Higher power, greater cost, lower yield, one- to two-generation process lag, sector erase. Concerns about data retention at operating temperatures higher than 85°C.
Logic-CMOS MTP	Kilobits	Leading process, no extra process steps, lower power consumption, portable to advanced processes	Smaller memory, slower reads, medium cell area
Fuse/antifuse OTP	100s of bits	Leading process, scalable	Higher power consumption, no field programmability, poor reliability
Logic-CMOS OTP	100s of kilobits	Leading process, portable, field programmable, small cell area	Smaller memory

option works unless the design calls for field programmability or testability. If this situation arises, the only choice is logic NVM. For the digital portion, using SONOS flash provides designers with a lower power, faster program option than embedded EEPROM. Selecting logic NVM for the midsized-memory requirements in the digital back end will cost you area and speed but will lower cost and typically increase yield. Now, the entire design fits into one process—generic logic CMOS—and requires no added process steps. Using generic logic CMOS provides designers with the additional advantages of leading-edge-process availability, design portability, and a lower power design. The only trade-off of this option is the limitation on memory size. If the microprocessor requires an MTP memory on the order of multiple megabits, for example, size constraints limit the choice to EEPROM or flash. **Table 3** summarizes the primary design trade-offs.

Another aspect designers should consider is support-circuitry overhead. All memories require operational control signals and decoding circuits, with complexity varying according to memory architecture. In the absence of external high-voltage lines, higher programming voltage requirements must have either on- or off-chip charge pumps. Designs that require greater memory endurance may require error-correction coding and some degree of cell redundancy. Depending on the erasure method the device uses, designers may need to use additional control circuitry to prevent overerase problems, such as stuck bits. Some designers may choose to use drop-in memory IP (intellectual property) from an IP vendor, which gives designers visibility into only the

Intersil Digital Light Sensors

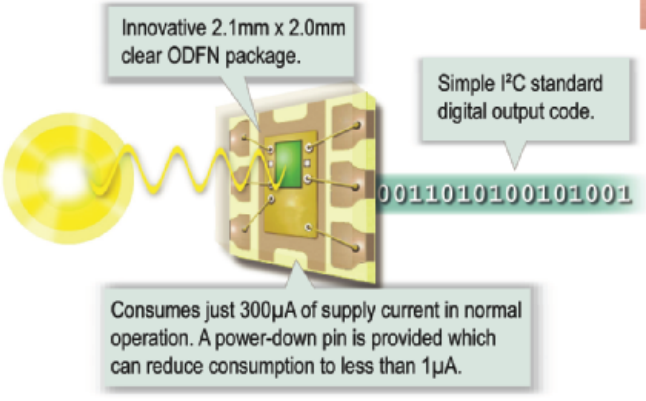
High Performance Analog

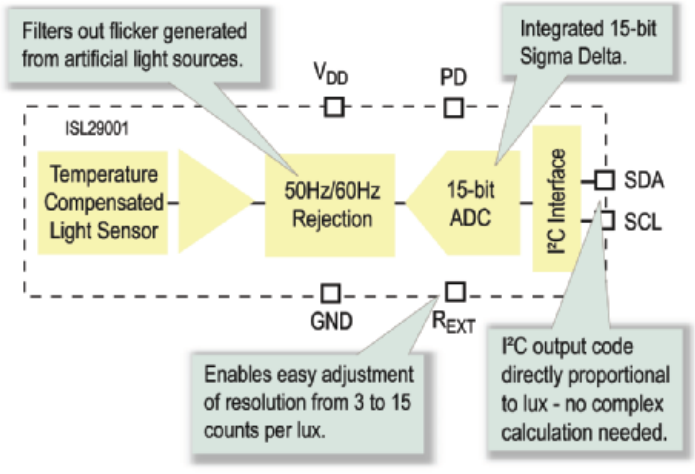


The Best Digital Light Sensor and Its Closest Competitor

With light sensitivity only matched by the human eye, Intersil's ISL29001 Digital Light Sensor provides simple, pure 15-bit I²C digital data.

Drawing less than 300µA of supply current, the ISL29001 provides 15-bit effective resolution. This state-of-the art device integrates two photodiodes and an ADC into a super small 2.1mm x 2.0mm ODFN package. The digital data in standard I²C format couldn't be simpler to use. It's no wonder **EDN Magazine** has selected one of this family's light sensors as a finalist for this year's **Innovation of the Year Award**.





ISL29001 Key Features:

- I²C interface produces simple I²C output code, directly proportional to lux
- 0.3 lux to 10,000 lux range
- 50Hz/60Hz rejection to eliminate artificial light flicker
- Human eye response
- 15-bit effective resolution
- Adjustable resolution: 3 to 15 counts per lux
- 2.5V to 3.3V supply
- Temperature compensated
- 6-pin ODFN (2.1mm x 2mm)
- Pb-Free plus anneal available (RoHS compliant)

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TABLE 4 SUPPORT-CIRCUIT IMPACT

Peripheral circuit	Usage example	Impact
Control circuits	Parallel versus serial input, decoding control	Routing area on-chip, complexity of controller, size of memory drop-in
Charge pump	Allows single-chip supply voltage by generating higher on-chip programming voltages	Area, power, not necessary to have internal if programming only once
Error-correcting code	Increases reliability of memory	Adds complexity and might not be needed for all applications

periphery of the memory. Designers care about the overhead because the selection of a type of NVM from a specific vendor impacts not only the chip design, but also the design and cost of the board it occupies. **Table 4** summarizes a few peripheral-support-circuitry considerations.

Moving from external NVM to an internal embedded approach provides many benefits: increased design accuracy, lower board costs, decreased board complexity, greater testability, the ability to correct design errors, field programmability, and increased security. If designers can fit the design into a generic logic-CMOS process using careful design partitioning, their design will gain additional benefits, including lower power consumption, lower chip costs, and the availability of both OTP and MTP NVM from a single IP supplier.

Designers should first consider the type and size of NVM their design needs. Once they understand the NVM requirements, they can then evaluate requirements for read speed, design portability, field programmability, power consumption, and design area versus cost. Armed with this information, designers can pick the best IP supplier for the application at hand. Understanding the NVM options could mean the difference between a design that works and a design that works but soon fails in the marketplace. EDN

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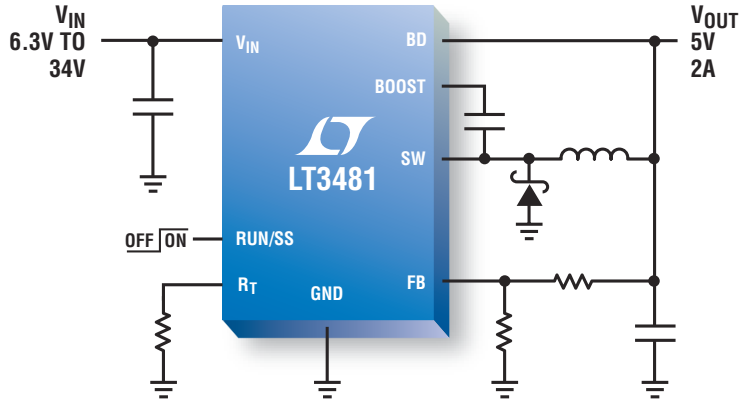
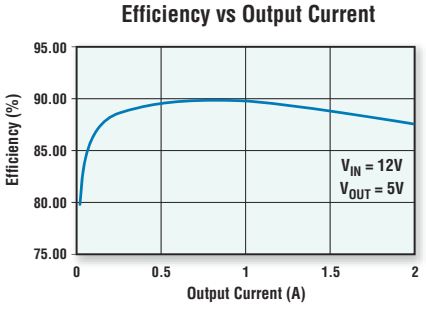
AUTHORS' BIOGRAPHIES

Ann De Vries is a senior technical writer at Impinj (Seattle). She received a master's degree in electrical engineering from the University of Southern California (Los Angeles) and a bachelor's degree in physics from the University of California—Riverside. Before joining Impinj, she held engineering-management and -design positions at General Instrument and TRW.

Yanjun Ma is a manager of technology development at Impinj (Seattle). He received his doctorate from the University of Washington (Seattle) and has since worked at Bell Labs, Sharp Labs of America, and Lattice Semiconductor. He has 20 US patents on semiconductor processing and devices and has published more than 60 journal articles.

36V Buck Converter Has It All





Actual Size
Demo Board

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The LT®3481 monolithic buck converter has everything needed to simplify mid-range input voltage step-down conversion designs. Its high switching frequency operation minimizes the size and cost of capacitors and inductor. Low ripple Burst Mode® operation typically has less than $15mV_{P-P}$ ripple at the output and a quiescent current of only 50µA. The internal 3.2A rated switch provides 2A of continuous output current at voltages as low as 1.27V. With its high level of integration and fast switching, a complete LT3481 solution occupies less than $1cm^2$.

Features

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- 2A Maximum Output Current
- Low Ripple Burst Mode Operation
  50µA at $12V_{IN}$ to $3.3V_{OUT}$
  Output Ripple < 15mV
- Adjustable Switching Frequency:
  300kHz to 2.8MHz
- Integrated Boost Diode
- Small 10-Pin Thermally Enhanced MSOP & 3mm x 3mm DFN Packages

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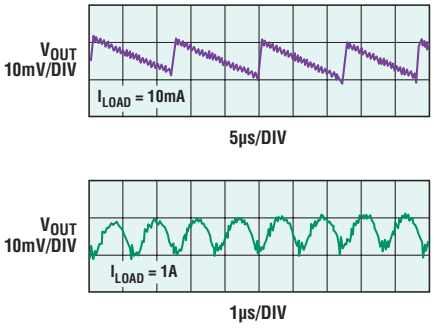
V_{OUT} = 3.3V, F_{SW} = 800kHz
C_{OUT} Just 22µF!



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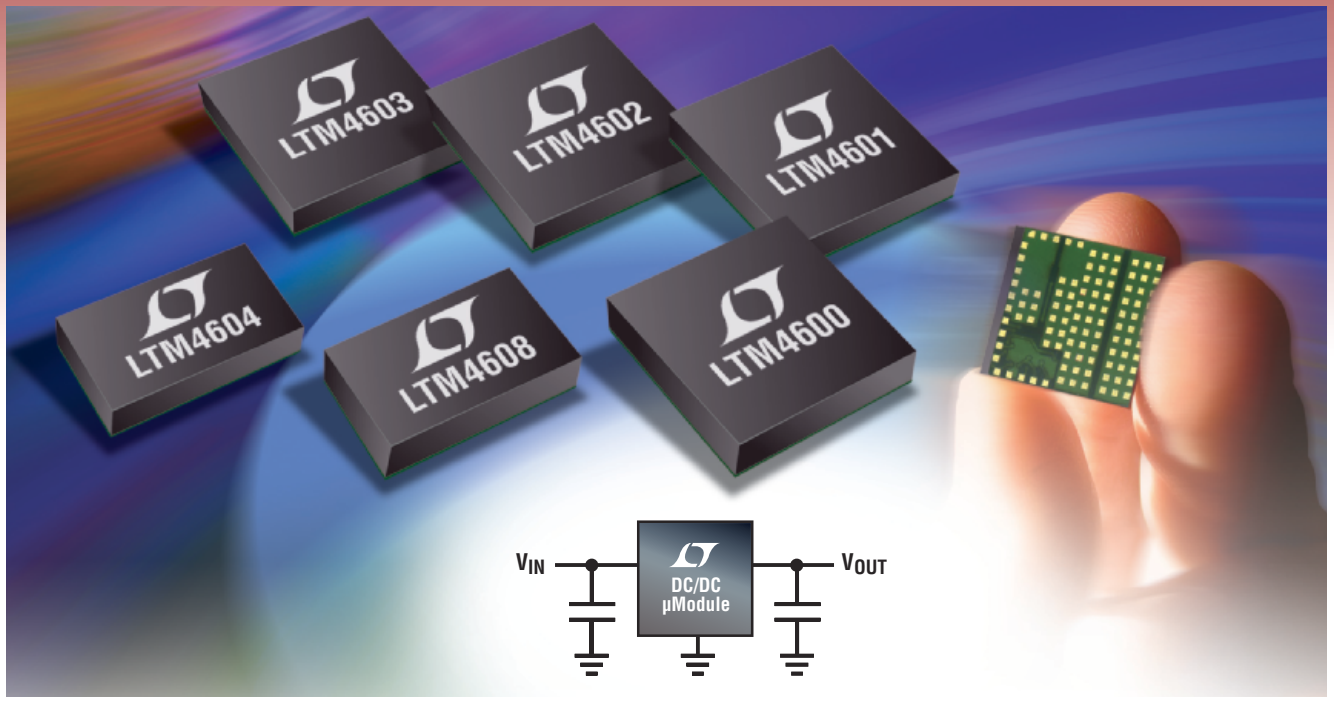

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New DC/DC µModule Family

V_{IN}: 4.5V-28V; V_{OUT}: 0.6V-5V						LGA Package	
Part No.	I_{OUT} (DC)	Current Share	PLL	Track, Margin	Remote Differential Sense	Height	Area
LTM®4602	6A	Combine two for 12A to 24A or 4x LTM4601 for ≤48A				2.8mm	15x15mm
LTM4603	6A		✔	✔	✔		
LTM4603-1	6A		✔	✔			
LTM4600	10A						
LTM4601	12A		✔	✔	✔		
V_{IN}: 2.5V-5.5V; V_{OUT}: 0.8V-3.3V							
LTM4604	4A	4x for 16A-32A	✔	✔		2.3mm	15x9mm
LTM4608*	8A		✔	✔	✔	2.8mm	15x9mm

*Future Product

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Microcontroller drives logarithmic/linear dot/bar 20-LED display

Dhananjay V Gadre and Anurag Chugh,
Netaji Subhas Institute of Technology, New Delhi, India

Available for more than 20 years, National Semiconductor's (www.national.com) venerable LM3914 dot/bar-display driver still enjoys wide popularity among designers. The LM3914 can sense an analog voltage level and display it on 10 LEDs by illuminating one of 10 in dot mode or by progressively illuminating LEDs in bar-graph mode. Recently, an application needed an analog-input-voltage display capable of displaying more than 10 levels in linear- and logarithmic-scale formats. According to the LM3914's data sheet, you can cascade multiple 3914s to display more than 10 levels (**Reference 1**), but, even so, the LM3914 offers only linear displays of its input voltage. (**Editor's note:** National Semiconductor also offers the LM3915, a logarithmic, 3-dB-per-step version, and the LM3916, which displays its input in volume units, for audio applications.)

This application required more flexibility than the LM3914 offers, and it uses a circuit based on an Atmel (www.atmel.com) AVR-family ATTiny13 microcontroller, which features 1 kbyte of program memory; a four-channel, 10-bit ADC; and six general-purpose I/O pins. Altering the circuit's firmware allows linear or logarithmic scaling of the 0 to 5V input-voltage range.

The circuit in **Figure 1** continuously displays the input voltage in 20 levels. When closed, switch S_1 freezes the displayed reading at its then-current level. Five of the microcontroller's six I/O pins control all 20 LEDs and the switch. Configured as an ADC-input channel, the remaining I/O pin receives the analog-input voltage. The microcontroller uses Charlieplexing, a method of using I/O lines to drive as many as N×(N−1) LEDs, to drive 20 LEDs with only five I/O pins (**references 2** through **4**).

The firmware is written in C and compiled using AVR-GCC, a freeware C compiler and assembler available in Windows and Linux versions at www.avrfreaks.net. It uses the Tiny13's internal 10-bit ADC operating in free-

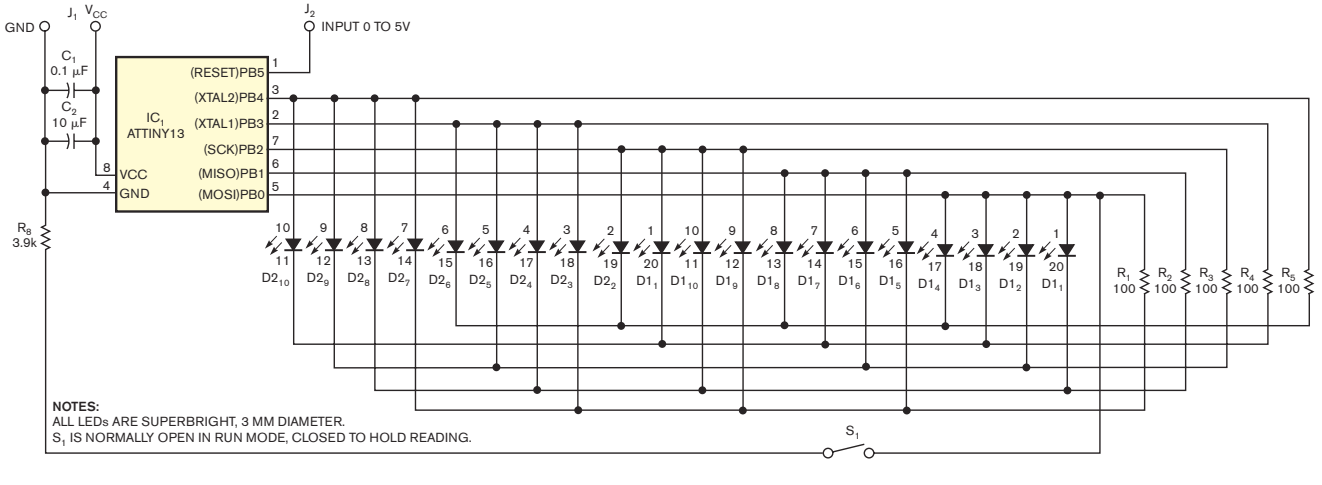

Figure 1 Based on a low-cost microcontroller, this dot/bar LED driver operates in linear or logarithmic modes.

running, interrupt-driven mode to convert the analog-input voltage into a digital number. Upon completion of each conversion, the ADC generates an interrupt that a subroutine reads; the interrupt stores the ADC's converted output in a shared variable.

To provide a flicker-free display, an internal timer generates a 1875-Hz interrupt derived from the 9.6-MHz system clock to drive the multiplexed LEDs at a rate exceeding 90 Hz. Dividing the ADC count by a constant yields a linear display of the input voltage. A look-up table scales the ADC count to produce a logarithmic display. **Figure 2** shows the logarithmic-conversion curve that defines the look-up table's values. Versions of the ATTiny13's control programs for linear and logarithmic scales are available for downloading from the online version of this Design Idea at www.edn.com/070118di1. You can modify the source code to display only a particular subrange of the input voltage of 0 to 5V. For example, you can specify a linear-display range spanning 1 to 3V or a logarithmic scale for input voltages of 2 to 3V. EDN

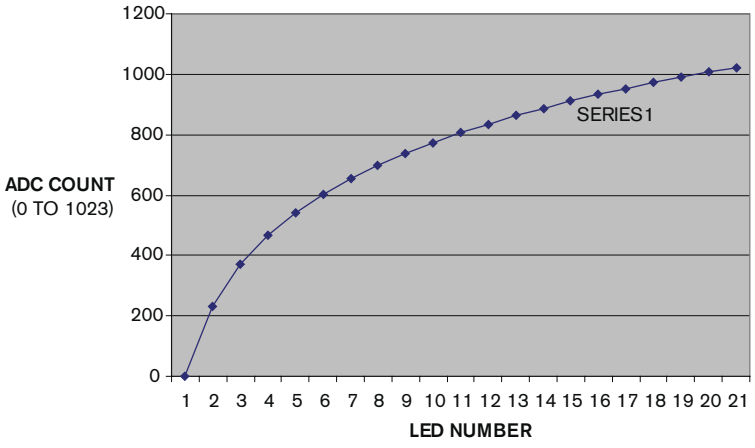

Figure 2 A linear-to-logarithmic-conversion curve defines the input voltage required to illuminate a particular LED.

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Optical feedback extends white LEDs' operating life

Bjoy Santos, Intersil Corp, Milpitas, CA

Regardless of its color, an LED's light output varies as a function of forward current and ambient temperature. As **Figure 1** shows, an LED's light output can vary by as much as 150% over its operating-current range. In response, a designer's first attempt to solve the problem focuses on driving the LEDs with a constant current. The most common white-LED-driver circuits use an inductor-based dc/dc boost-converter topology similar to the circuit in **Figure 2**. A current-feedback controller ensures that the voltage across current-sensing resistor R_1 remains constant. As a result, the controller varies the voltage across the entire string to maintain the LEDs' current constant without regard to

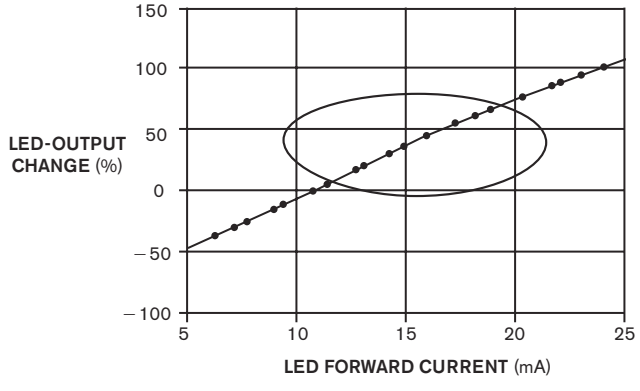
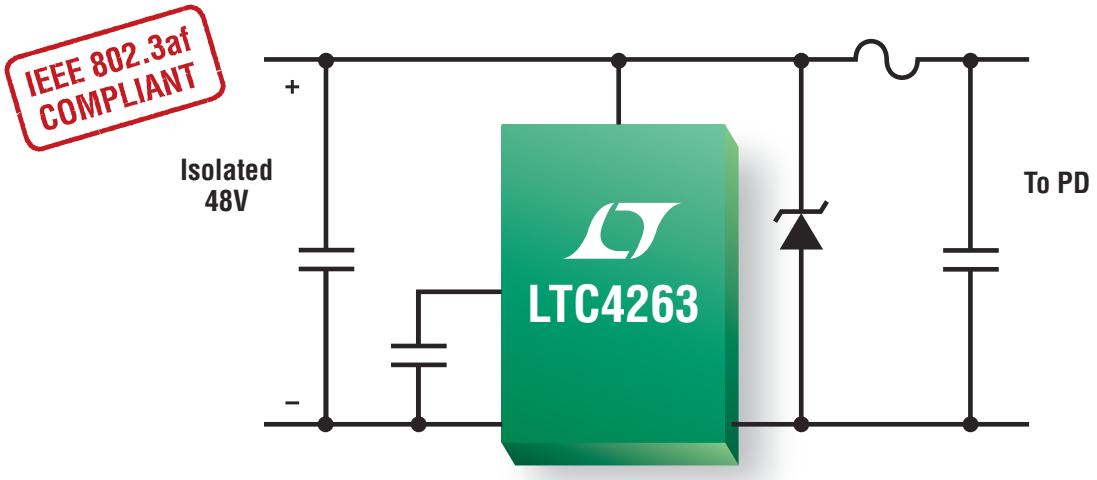


Figure 1 An LED's light output changes considerably as a function of its forward current, even within the sweet spot (oval area) of its nominal operating current.

Single Port PoE



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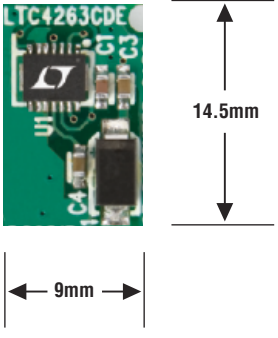
Small Footprint, Simple Design



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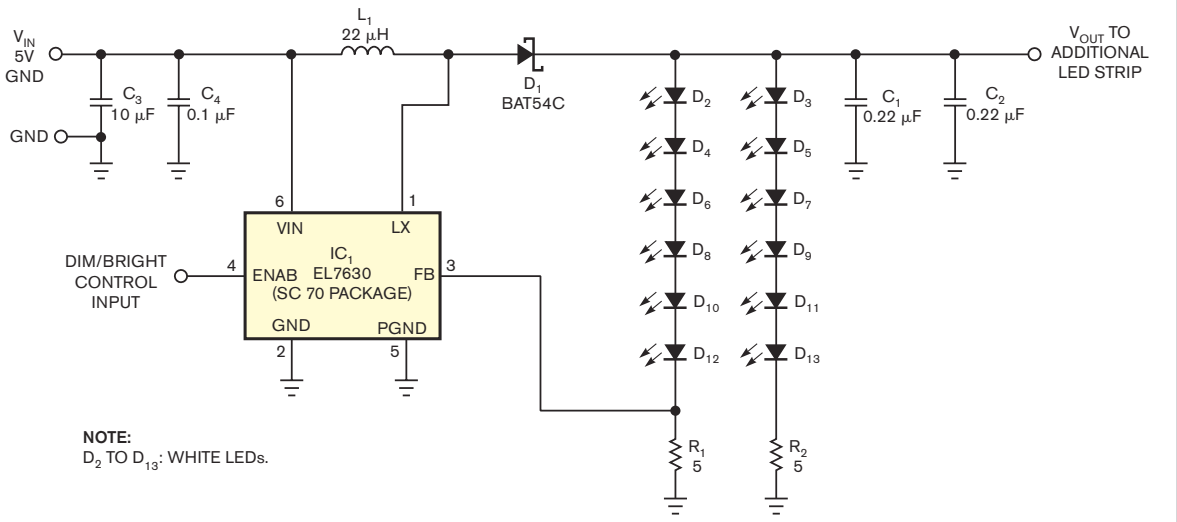
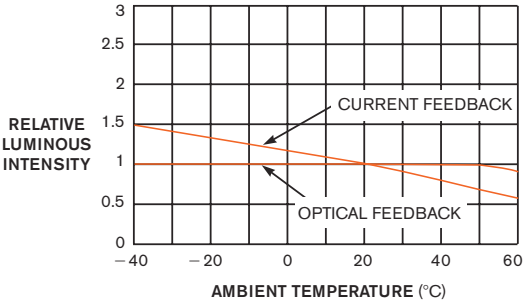


Figure 2 One method of driving an LED illuminator samples current through a string and adjusts the voltage across the entire string to maintain a constant current.

the LEDs' actual light output.

Driving series-connected white LEDs with a current source relies on the assumption that, at constant current, an LED's light output remains constant. Unfortunately, all LEDs exhibit a nonlinear decrease in brightness as a function of operating time. Although less obvious in colored LEDs that find use as indicators, the decrease in brightness of a white-LED-illuminator-array source becomes noticeable over an extended period. Brightness also varies as

Figure 3 Even at a constant forward current, an LED's light output correlates strongly with temperature and can vary by as much as 100% over the entire operating-temperature range (upper curve).



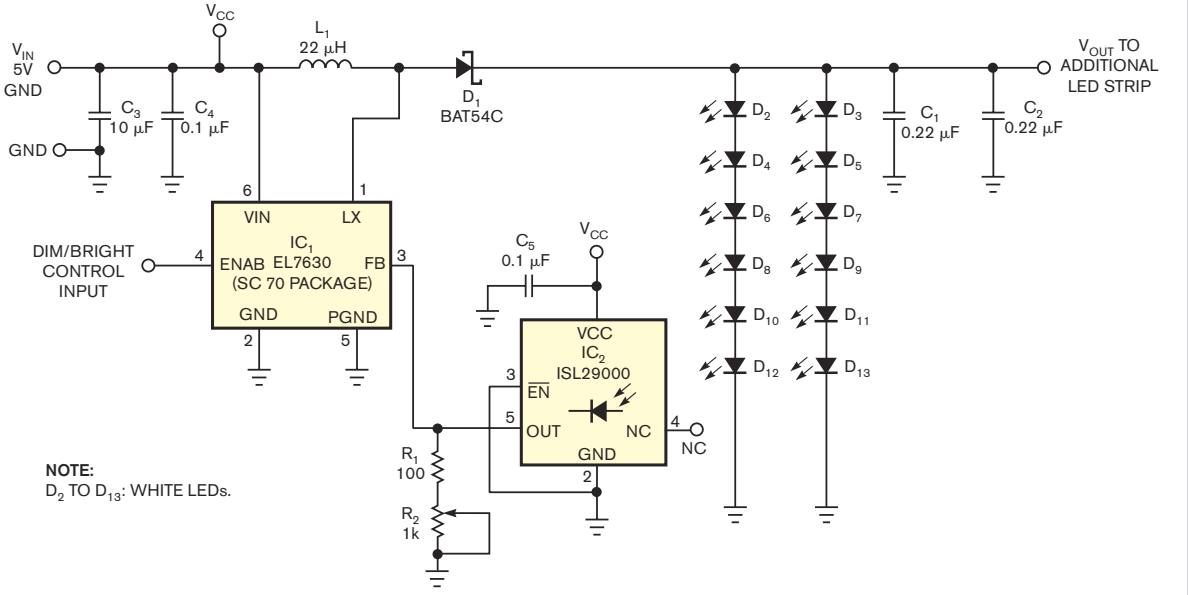


Figure 4 Photosensor IC_2, an Intersil ISL29000, resides near an LED to detect brightness fluctuations and provides compensating feedback to IC_1, the current controller, which is an Intersil EL7630 pulse-width regulator.

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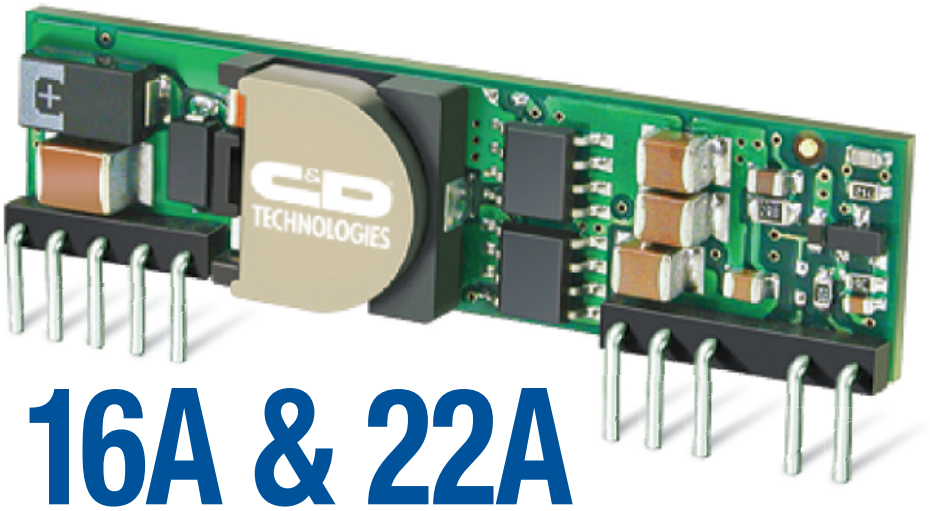

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Output Current	Input Voltage		Output Voltage	Untrimmed VOUT Accuracy	R/N Max.	Efficiency	Package Size	Datasheet at www.cd4power.com
	Nom.	Range						
A	Vdc	Vdc	V	%	mVp-p	%	Inches	
6	5	2.4 to 5.5	0.75 to 3.3	±2	25	94	Vertical Models 2x 0.36 x 0.5h Tyco Compatible 2 x 0.37 x 0.5h Horizontal Models 2 x 0.5 x 0.37h	**LSN2-T/6-W3**
6	12	8.3 to 14	0.75 to 5	±2	25	93		**LSN2-T/6-D12**
10	3.3	3 to 3.6	1 to 2.5	±1	35	90.5 to 95.5		**LSN-10A, D3**
10	5	2.4 to 5.5	0.75 to 3.3	±2	25	95		**LSN2-T/10-W3**
10	5	4.5 to 5.5	1 to 3.8	±1	35	89 to 96		**LSN-10A, D5**
10	12	8.3 to 14	0.75 to 5	±2	75	95		**LSN2-T/10-D12**
10	12	10.8 to 13.2	1 to 5	±1.25	45 to 75	86 to 95.5		**LSN-10A, D12**
16	5	2.4 to 5.5	0.75 to 3.3	±2	50	95		**LSN2-T/16-W3**
16	3.3/5	3 to 5.5	0.75 to 3.3	±1.5	50	86 to 95		**LSN-16A, W3**
16	12	8.3 to 14	0.75 to 5	±2	75	94		**LSN2-T/16-D12**
16	12	10 to 14	0.75 to 5	±1.25	45 to 75	86 to 95.5		**LSN-16A, D12**
22	12	8.3 TO 14	0.75 to 5	±2	90	95		**LSN2-T/22-D12**

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a function of temperature, which can affect an illuminator's performance over an extended-temperature range (upper curve, **Figure 3**).

To compensate for LED-output variations due to aging and temperature fluctuations, the control loop needs more information in addition to voltage or current data. Adding an ambient-light sensor and optical feedback to the control loop can ensure that a white LED's light output remains uniform and consistent over time and temperature variations. An optical sensor can measure the LED's light-output intensity and provide a feedback signal for the control loop, which can adjust the current to produce a relatively constant light output. As the LEDs' light outputs decrease, increased current compensates for aging and temperature-induced variations (lower curve, **Figure 3**).

The circuit in **Figure 4** includes an optical-feedback loop based on Intersil's (www.intersil.com) ISL29000 light-to-current optical sensor, IC_2, which senses changes in the LEDs' light output and decreases the feedback voltage applied to IC_1, the current controller, an Intersil EL7630. The pulse-width-modulated controller then increases the LED-drive current's duty cycle, boosting the LED current until the feedback voltage reaches its nominal value. As ambient temperature decreases, the LEDs' light output tends to increase, and IC_2 delivers a higher feedback voltage to the controller, which responds by lowering the duty cycle to decrease the LEDs' current and thereby compensates for the decrease in temperature. EDN

Sequencer controls power supplies' turn-on and turn-off order

Eric Schlaepfer, Maxim Integrated Products Inc, Sunnyvale, CA

When a design based on multiple point-of-load dc/dc converters requires a specific power-supply-start-up sequence, wiring each converter's power-good output to the next converter's enable input produces the desired voltage cascade. Although this approach works well for simple designs, it fails to satisfy a requirement of many modern microprocessors and DSPs: that, during shutdown, the power-supply rails switch off in reverse order. Although various vendors provide programmable-sequencing ICs, these components are usually too expensive for cost-sensitive applications.

Offering an alternative to programmable-sequencing ICs, the circuit of **Figure 1** can sequence and cheaply

(continued on pg 92)

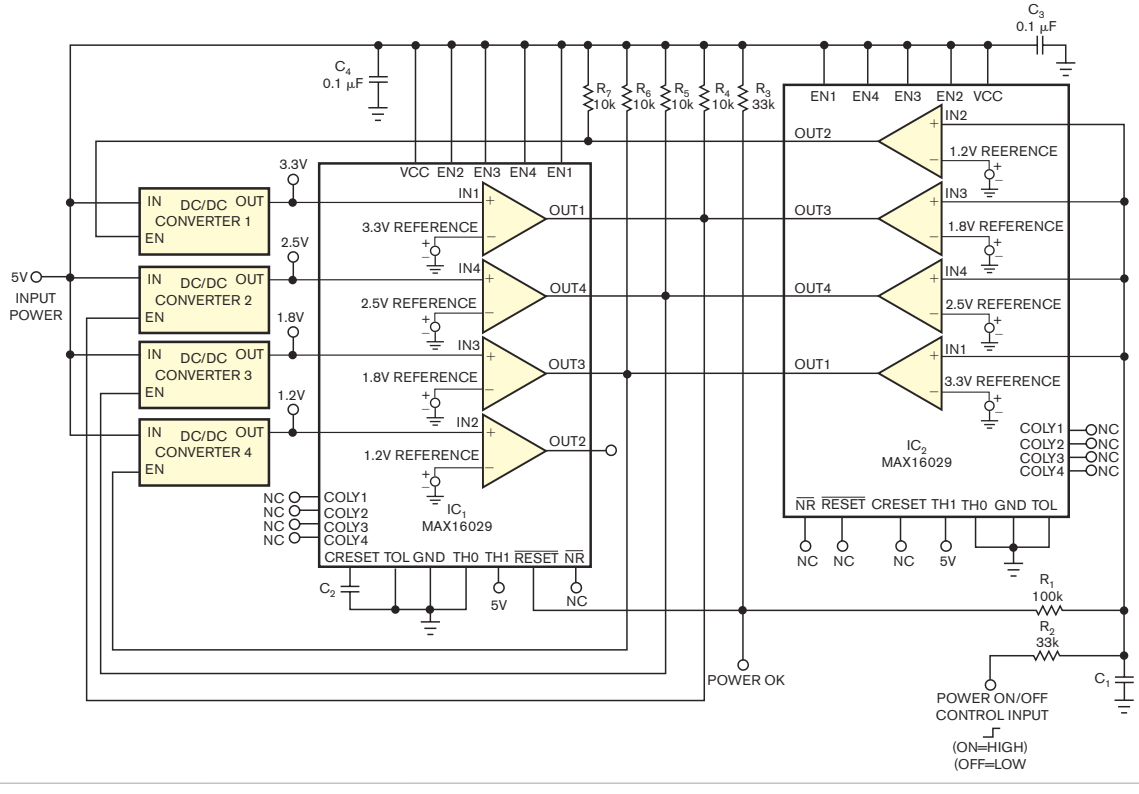

Figure 1 Comprising a pair of inexpensive ICs, this circuit applies four supply voltages in a specified order at power-up and then removes them in reverse order at power-down.

LINEAR TECHNOLOGY

DESIGN NOTES

Dual Current-Sense Amplifiers Simplify H-Bridge Load Monitoring

Design Note 407

Jon Munson

Introduction

The H-bridge power-transistor topology is increasingly popular as a means of driving motors and other loads bi-directionally from a single supply potential. In most cases there is great benefit in monitoring the current delivered to the load and utilizing this information in real-time to provide operational feedback to a control system. In most new designs, pulse-width-modulation (PWM) techniques are used to provide highly efficient variable power-delivery, but this places extremely fast voltage transitions at both terminals of the load and therefore complicates the instrumentation problem. New high side current sense amplifiers from Linear Technology can simplify this problem.

Measuring Load Current in the H-Bridge

The classical approach to load monitoring is to place a small value sense-resistance in series with the load that can develop a measurable voltage drop representing the load current (see Figure 1). The difficulty here is that with PWM activity, the common mode voltage at the sense resistor has nasty voltage transitions that can corrupt the sense amplifier operation with high frequency hash. While this hash can be filtered to recover useful low frequency information, the ability to provide fast fault protection is then lost. Additionally, this "flying" sense resistor configuration is unable to monitor switch shoot-through current, leaving many important fault modes undetected or unmanaged (failed switch function, for example).

A far more practical method is to monitor the supply current fed to each half-bridge as shown in Figure 2. This scheme provides several benefits that simplify and improve the circuit performance. The main improvement comes from having the sense resistors at a relatively constant common mode voltage (i.e., the power supply voltage) so that fidelity of the PWM current waveform can be preserved. Additionally, by monitoring each half-bridge individually at the supply side, both failed power device operation and load shorts to ground are readily detected and manageable.

By using PWM logic that generates "sign-magnitude" control, one of the half-bridges is in a 100% pull high condition (depending on the direction or polarity of drive). The load current equals the current delivered through the 100% (fully on) switch, unaffected by the duty cycle of the PWM activity on the other half-bridge. This permits simple reconstruction of the load current waveform using suitable high side sense amplification techniques.

The Simple Solution

The LTC6103 and LTC6104 dual high side sense amplifiers are ideal for performing the H-bridge monitoring function. Both parts include two current sense input channels and

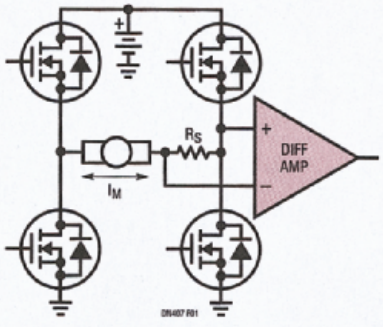

Figure 1. Classical Load Sensing Problematic with PWM

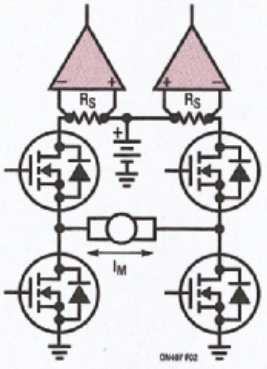

Figure 2. PWM-Compatible H-Bridge Load Sensing

furnish either two unidirectional outputs (LTC6103) or a single bidirectional output (LTC6104). Since each current sense channel operates in a unidirectional fashion, only the current from the fully on half-bridge is monitored.

Since the current pulses in the other half-bridge are in the opposite direction, that amplifier channel remains in a cutoff condition and does not impact the reading. This means that the output signals only reflect the fully-on half-bridge current, which is identical to the controlled load current.

With their fast (microsecond level) response times, these parts also offer overload sensing, thereby providing the ability to signal power device protection circuits in the event of fault conditions. Both parts are furnished in tiny MSOP-8 packages for compact layouts and can operate with up to 60V power supply potentials. With their 70V transient capability, the need for additional surge suppression components is eliminated in harsh automotive applications.

The dual outputs of the LTC6103 can be used individually to provide overload detection, and/or may be taken as a differential pair to provide a bidirectional signal to an analog-to-digital converter (ADC) for example. Figure 3 shows a typical circuit for a generic H-bridge application. The power devices may be complementary MOSFETs, pure N-MOSFETs, or other switching devices. When the bridge drives the load (a motor assumed in the example shown), one of the LTC6103 outputs rises above ground, while the other remains pulled down to ground, thereby forming an accurate bidirectional differential output with a common mode voltage that never falls below ground. The selection of output resistance (4.99k in the example) can be scaled to satisfy the source-impedance requirement of any ADC.

As an alternative, the output structure of the LTC6104 provides a single bidirectional signal. The output connection can either source or sink current to a load resistance, depending on which input channel is sensing current flow. A negative-going output swing remains linear as long as Pin 4 (V^-) is lower than the lowest expected output level by at least 0.5V. This condition is met if the load resistance is returned to a suitable reference voltage while Pin 4 is grounded (as shown in the Figure 4 example). The output resistance could also be returned directly to ground to form a true bipolar output if Pin 4 is tied to a suitable negative supply, such as –3V.

Conclusion

Designing a load current monitor for an H-bridge power driver is not difficult if you have the right amplifier. The LTC6103 and LTC6104 fit the bill. They include dual sense inputs and a choice of two different output configurations—features that reduce complexity and printed circuit area.

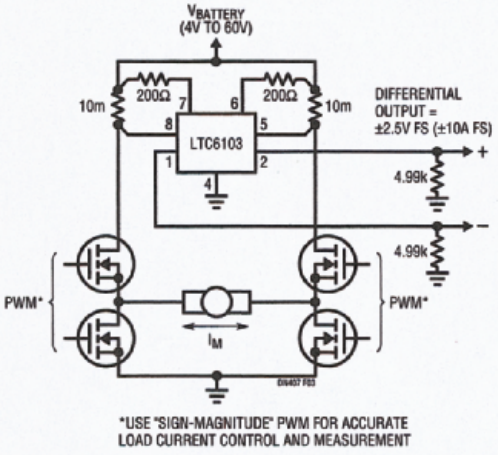

Figure 3. LTC6103 Provides Bidirectional H-Bridge Monitoring with ADC-Friendly Differential Output

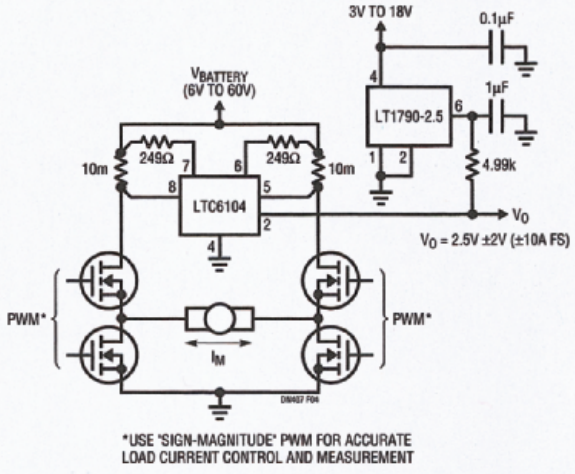

Figure 4. LTC6104 Provides Bidirectional H-Bridge Monitoring with Single-Ended Output

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(continued from pg 88)

and effectively monitor four power-supply rails. Four dc/dc power supplies provide the application circuit with 3.3, 2.5, 1.8, and 1.2V. A quad supervisor circuit, IC_1, monitors each rail, generating the master POK (power-OK) signal and ensuring that, during power-up, the next supply in the sequence does not turn on until the preceding supply voltage is valid. Using an RC circuit comprising R_1, R_2, R_3, and C_1, a second quad supervisor, IC_2, creates the power-up and power-down sequences. Each supervisor's internally preset voltage threshold eliminates the need for external resistive-voltage dividers.

Connecting the power-on/off signal to 5V initiates a power-up sequence, which charges C_1 through R_2. As the capacitor's voltage gradually exceeds 1.2, 1.8, 2.5, and 3.3V, each of IC_2's corresponding open-drain outputs floats, thereby allowing the power supplies to turn on in the prescribed sequence. After a time delay, which C_2 sets, and after all four supplies turn on, the POK signal asserts—that is, goes high.

To monitor the supply rails, allow the power-on/off-control input to float. Resistors R_1 and R_3 sustain the voltage across C_1 and maintain the POK signal high to keep the power supplies on. When an output-voltage fault occurs, POK rapidly deasserts, discharging C_1 through R_1 and shutting off all of the power supplies. To remove power in an orderly sequence, connect the power-on/off signal to ground. Capacitor C_1 discharges through R_2 and also through R_1 when POK deasserts, turning off each power supply in reverse order (**Figure 2**).EDN

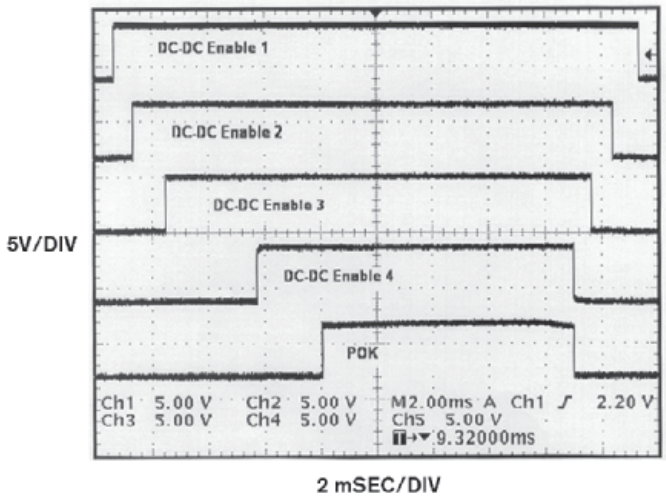

Figure 2 Beginning with a dc/dc converter, the circuit in Figure 1 switches on three additional converters in sequence and generates a POK signal. Pulling the circuit's on/off input low removes the POK signal and switches off all four converters in reverse order.

Use dual op amp in an instrumentation amp

Jerald Graeme, Burr-Brown Corp, Tucson, AZ

Editor's note: *Here's an oldie but goodie. EDN editors regularly field requests for copies of articles that predate our online archives (www.edn.com/archives). But this Design Idea from our Feb 20, 1986, issue has generated many more requests than normal. We aren't sure how readers know of this Design Idea, but its enduring popularity has led us to publish it once again, and now it will be available in our online archives.*

Although monolithic instrumentation amplifiers are more cost-effective than their discrete and modular predecessors, the limited variety of monolithic instrumentation amps restricts their use. You can widen your options, however, by deriving the differential response of an instrumentation amplifier from a dual op amp (**Figure 1**). The circuit uses FET-input op amps to provide lower noise and lower input-bias currents than monolithic instrumentation amps can offer.

In **Figure 1**, feedback networks for the two op amps are interconnected to establish IC_{1B} as an inverting amplifier in the feedback path of IC_{1A}. Each amplifier provides an external signal input with the high impedance expected of an instrumentation amplifier. (Input-bias currents for this circuit are 2 pA at 25°C.)

Feedback from each amplifier forces a voltage $(V_1 - V_2)$ across the gain-setting resistor R_G. Signal current in the combined feedback path is thus proportional to the differential input voltage and inversely related to R_G. The output voltage, V_{OUT}, equals $G(V_1 - V_2)$—that is, $V_{OUT}=2(1+R/R_G)(V_1 - V_2)$.

You choose R_G for the desired gain G, which may range from a value of 2 (R_G omitted) to a maximum that is limited only by the op amps' open-loop gain, the allowable gain error, and the required bandwidth. The **Figure 1** circuit provides a 2-kHz bandwidth at a gain of 2000; in general, the bandwidth is about 2 MHz/G. What's more, the output offset equals the difference in op-amp offsets multiplied by G.

The dc CMR (common-mode rejection) is an important spec for instrumentation amps; in **Figure 1**, CMR depends primarily on matching values for the four resistors labeled R. DC CMRR

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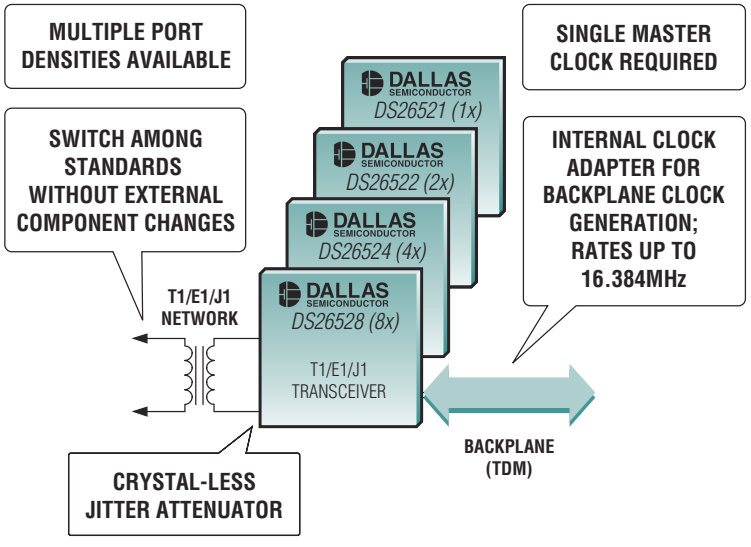

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(common-mode rejection ratio) is the reciprocal of the net fractional resistor mismatch; that is, 10,000-to-1 (−80 dB) for a 0.01% mismatch. AC CMR, on the other hand, is limited by the op amps' unequal feedback factors. The network within the shaded region lets you compensate for the effect of unequal feedback factors where necessary—in applications in which the frequency of common-mode voltage exceeds the useful frequency range for signals.

Finally, note that op amp IC_{1B}'s output (the combined differential and common-mode signals) has a wider swing than V_{OUT}. Consequently, this output—equal to $2V_1+(R/R_G)(V_1-2V_2)$—must remain within the op amp's common-mode range to ensure linear operation. EDN

Correction: In the print version of the Dec 15, 2006, Design Idea "Magnetic-field probe requires few components," we inadvertently omitted the byline of one of the Design Idea's primary authors: Sandeep M Satav. You can read this Design Idea and see the correct bylines online at www.edn.com/article/CA6399102. We apologize for the error.

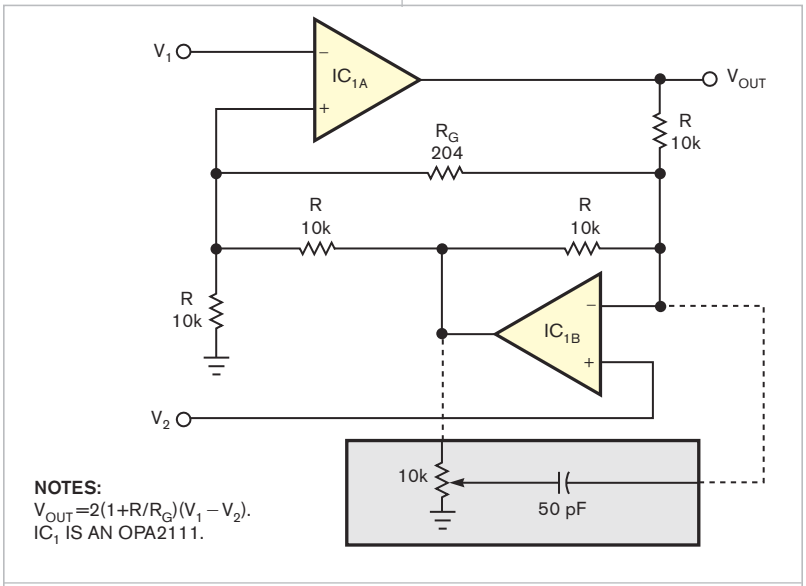

Figure 1 You can build an instrumentation amplifier by providing a common feedback path for the two sides of a dual op amp.

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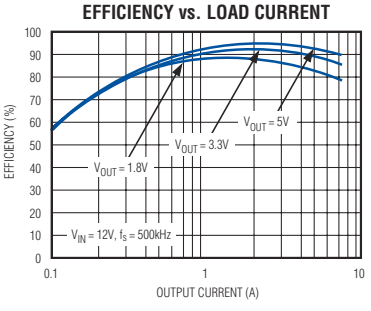

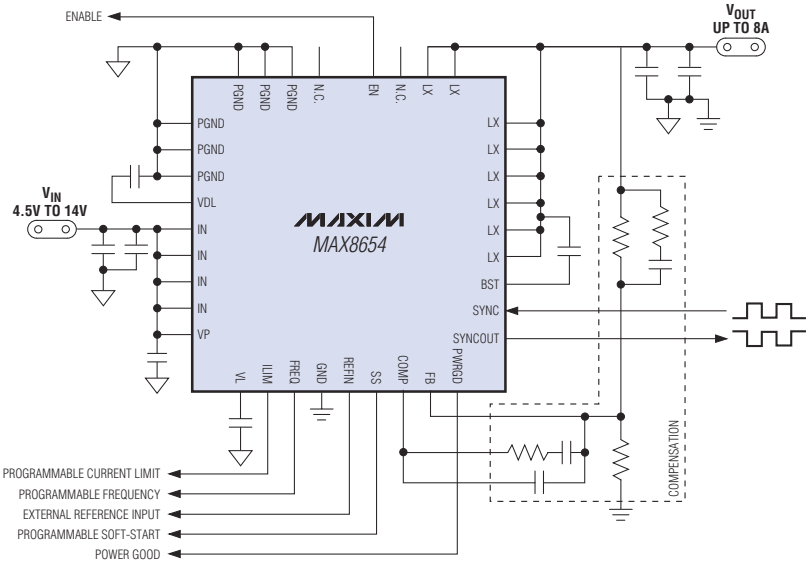

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LEDtronics, www.ledtronics.com

Charge pump combines dual low-dropout regulators and serial interfaces

Targeting portable systems using lithium-ion/polymer batteries, the 600-mA AAT2842 charge pump combines dual low-dropout linear regulators and serial-digital interfaces, providing independent control of LED functions. Two S²Cwire (Simple Serial Control) serial-digital interfaces allow designers to independently drive four LEDs for backlight display or keypad applications and four LEDs for high-current flash applications. The AAT2842 costs $1.75 (1000).

Advanced Analogic Technologies, www.analogictech.com

Fiber-optic LED transmitters have an 850-nm GaAlAs LED

The OPF670 optical-coupling series of fiber-optical LED transmitters allow integration into data-communications equipment. This LED-transmitter family includes the OPF670 in a TO-46 package, the OPF672 in a standard-profile metal package, and the OPF673 in a low-profile metal package. The devices can launch optical power into 50/125- or 62.5/125-micron-diameter, multimode fibers and comprise an 850-nm GaAlAs (gallium-aluminum-arsenide) LED. Prices for the OPF670 series range from $5.75 to $12.25 (1000).
Optek Technology, www.optekinc.com

Digital optocoupler suits hybrid-electric vehicles

Targeting hybrid-electric vehicles, the 10-Mbaud ACPL-M61T digital-interface optocoupler supports requirements of networking-, communication-, and system-management applications. The high-speed optocoupler features an enhanced wire-bonding process and an improved lead frame, improving reliability and heat dissipation. A high common-mode-rejection ratio provides high immunity to transient noises, EMI, and ground-loop eliminations. Offering a −40 to +125°C temperature range, the ACPL-M61T costs $2.50 (10,000).
Avago Technologies, www.avagotech.com

LED-driver controller targets rapid LED-current transients

Aiming at rapid LED-current transients as high as 20A/msec and a 30-kHz dimming frequency, the MAX16818 LED-driver controller targets projection and lighting applications. Average current-mode control, synchronous gate-drive circuitry, and a wide switching-frequency range allow the device to drive high-power LEDs in light sources including projectors, home-theater systems, rear-projection TVs, and automotive- and industrial-lighting fixtures. Available in a 5×5×0.8-mm TQFN-28 package, the MAX16818ETE+ costs $1.82.
Maxim Integrated Products, www.maxim-ic.com

productroundup

OPTOELECTRONICS/DISPLAYS

LED ballaster drives 24 LEDs

Delivering uniform LED brightness, the LT3003 LED ballaster drives three strings of eight LEDs each at a 3%-accurate current matching. Operating on a 3 to 40V input-voltage range, the device drives 24 LEDs at 350 mA each and features a 3000-to-1 dimming capability. The devices operate in buck, boost, and buck-boost modes. Buck-boost mode allows LEDs to return to the input supply in applications with an input supply that varies above and below the output voltage of the LED strings. The LT3003 costs $1.16 (1000).

Linear Technology, www.linear.com

COMPUTERS AND PERIPHERALS

Controllers, adapter connect devices to desktop

The IDE JBOD/RAID (just a bunch of disks/redundant array of inexpensive disks) PCIe (PCI Express) controller adds an extra channel, RAID capability, and JBOD capability to any desktop system, and you can install it in the PCIe slot of either a standard-height or a low-profile PC. The firmware enables setup of the two hard drives as RAID 1 for real-time backup, as RAID 0 for high performance, or as JBOD to combine the capacity of the two hard drives into one large volume. The USB 2.0-to-eSATA (External Serial Advanced Technology Attachment) adapter is compatible with port multipliers. The PCIe ExpressCard controller provides a way to add an ExpressCard socket to any desktop. The IDE JBOD/RAID PCIe controller and the USB 2.0-to-eSATA adapter cost $29.95 each. The PCIe ExpressCard controller costs $32.95.

Addonics Technologies, www.addonics.com

DVD-RAM drive features a high-speed USB interface

Measuring 5.43×6.38×0.87 in. and weighing less than 1 lb, the PX-608U portable DVD±R/RW CD-R/RW drive has a 2-Mbyte buffer and buffer-underrun-proof technology. The device supports 5× DVD-RAM and offers as much as 9.4 Gbytes of storage per double-sided disc. The device also has recording speeds of 8× DVD±R on single-layer media and 4× DVD±R on double- and dual-layer media. The drives support 8× DVD+RW, 6× DVD+RW, 8× maximum DVD-ROM, and 24× CD-R/RW/ROM. The PX-608U costs $199.99.

Plextor, www.plextor.com

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Samsung, www.samsung.com

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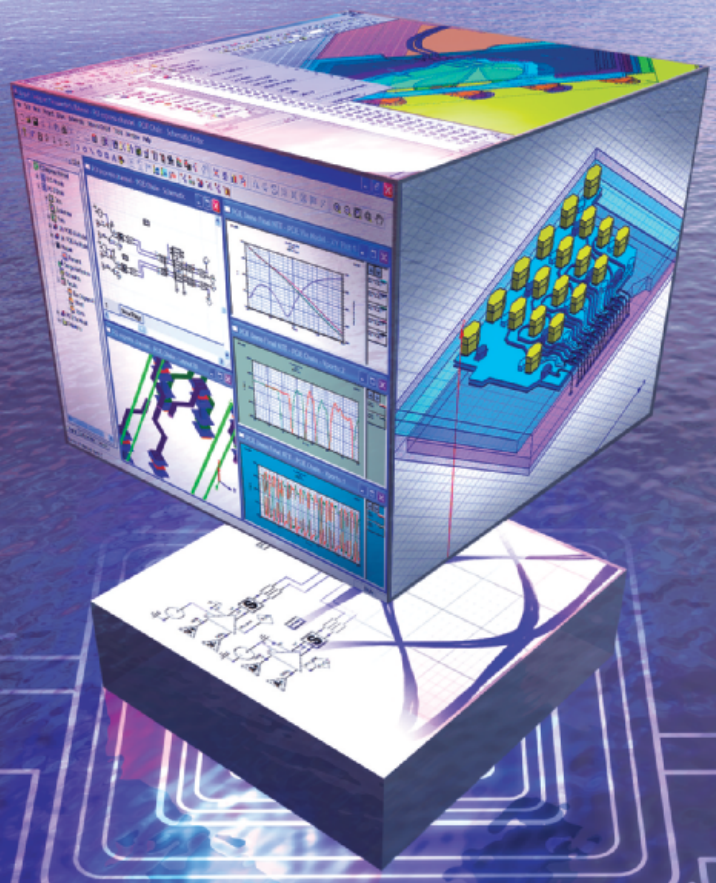

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Iomega Corp, www.iomega.com

1-Tbyte external-storage system has two RAID options

Shipped in the RAID (redundant array of inexpensive disks) 0 setting, the user-serviceable My Book Pro Edition II consumes less than 26 in.^{2} of desk space and includes EMC Retrospect Express Version 7.5 backup and system-recovery software. Users can set the device to reserve half of its capacity to mirror users' data in real time using the RAID 1 setting. The device also has FireWire 800, FireWire 400, and USB 2.0 interfaces. The My Book Pro Edition II costs $549.
Western Digital Corp, www.westerndigital.com

Monitor has high NTSC color gamut

Featuring nearly 100° of NTSC color gamut for CCFL (cold-cathode-fluorescent-lamp) displays, the 19-in. SyncMaster has a 2000-to-1 contrast ratio. The TFT (thin-film-transistor) LCD monitor also offers a 2-µsec response time. The SyncMaster 931C costs $299.99.
Samsung, www.samsung.com

Cards have effective data rate of 2 GHz

With a 2-GHz effective data rate, the Radeon X1950 XTX and X1950 CrossFire Edition graphics cards employ GDDR4 (series four of graphics-double-density-rate) memory technology. The X1950 series cards each cost $449.
ATI Technologies, www.ati.com

Monitor integrates down-firing speakers

Offering a 5-msec response time, the LCD-195WVXM monitor features a 1440×900-pixel native resolution and comes in a black cabinet. The LCD195WVXM monitor costs $284.99.
NEC Display Solutions, www.necdisplay.com

TEST AND MEASUREMENT

In-circuit emulator has easy-to-use GUI

Supporting development of embedded-system applications based on the vendor's TLCS-870/C series microcontrollers, the in-circuit RTE870/C light emulator includes debugger software with an easy-to-use interface. The software allows developers to quickly identify and fix software problems by setting breakpoints and event triggers, stepping through code, and activating trace functions with 1280-frame capacity. A timer function provides 1 µsec of resolution for 71 minutes and 100 nsec of resolution for seven minutes. The RTE870/C light emulator costs $800.
Toshiba America Electronic Components, www.toshiba.com

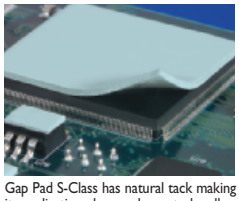
Debugging emulator replaces previous model

The on-chip E8a debugging emulator replaces the vendor's previous E8 model. The tool allows C source-level debugging with an M16C, H8/Tiny, or H8/Super-low power series microcontrollers, operating at full speed in the system. Developers of embedded systems can also combine the device with the FDT (flash-development-tool-kit) software for use as a programmer for loading code into the internal flash memory in most of the vendor's microcontroller families. The E8a emulator comes with a USB-interface cable, a user-interface cable, and interface software and costs $125.
Renesas Technology America, www.renesas.com

Thermal Challenge: VRM

High Ambient / High Watt Dissipation / Low Air Flow

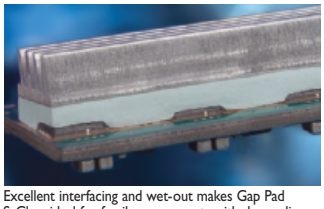
Solution: Bergquist S-Class Gap Pad®



Gap Pad S-Class has natural tack making its application clean and easy to handle.

Gap Pad S-Class is perfectly suited for high performance applications such as VRMs, BGAs and ASICs.

Bergquist's S-Class material is the perfect combination of softness and high thermal conductivity. With a low bulk Shore (00) hardness range from 20 to 30 and thermal conductivity from 2 to 3 W/m-K, these materials conform to demanding contours while maintaining their structural integrity. They are an ideal gap filling solution for applications with fragile components that can be damaged by higher mounting pressures. Gap Pad S-Class is also an excellent solution for CD/DVD drives, memory modules, and PC boards to chassis.



Excellent interfacing and wet-out makes Gap Pad S-Class ideal for fragile components with demanding contours and stack-up tolerances.

Ultra soft S-Class integrity offers easy application.

Gap Pad S-Class has a natural tack that eliminates the need for additional adhesive layers that can inhibit thermal performance. Its super soft, yet elastic nature provides excellent interfacing and wet-out, even to surfaces with high roughness or topography. Gap Pad S-Class features an embedded-fiberglass reinforcement that makes it puncture, shear and tear resistant. No tearing, flaking or crumbling – just clean and easy handling during the assembly process.

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Visit our web site or call to qualify for your FREE S-Class swatch kit with product details.

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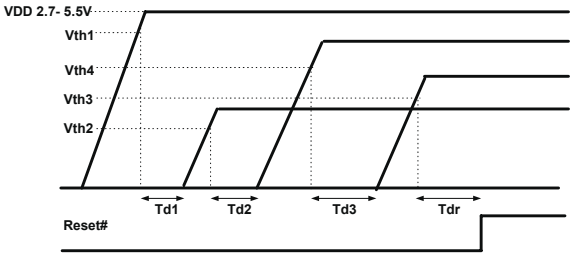
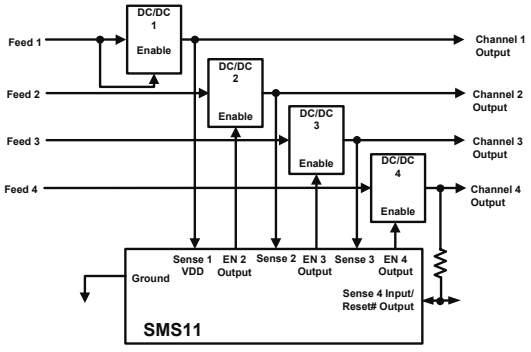




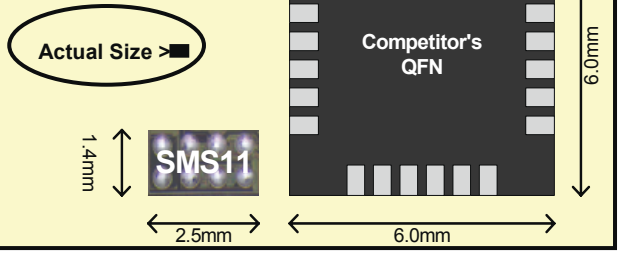
Shipped with your "custom parameters" already programmed. No extra manufacturing steps!

Single Summit device adjusts to many voltages and time delays; outperforms dozens of "fixed" competitor part numbers!

SMS11 Quad Sequencer/Reset

	SMS11	LTC2924	ISL612x	MAX687x
EEPROM Programming?	Y	N	N	Y
# of EN Outputs	4	4	4	5
# of Voltage Monitors	4	4	4	4
Voltage Monitor Threshold	Prog	Resistors	Resistors	Prog
Sequencing Order/Delay	Prog	Capacitor	Capacitor	Prog
Reset Timeout	Prog	Capacitor	Capacitor	Prog
# External components	0	13	17	5
Typ. Oper. Current (uA)	200	1500	140	1800
Package Type	CSP-8	SSOP-16	QFN-24	QFN-36
Package Size (mm)	1.4x2.5	6x5	4x4	6x6
Price $ (1K est.)	$ 2.00	$ 2.65	$ 2.87	$ 6.39

World's smallest quad sequencer!

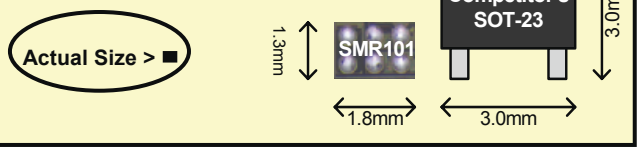


Summit Advantage

SMR101 Dual Reset

	SMR101	LTC295x	ISL8801x	MAX644x
EEPROM Programming?	Y	N	N	N
# of Reset Outputs	2	1	1	2
Reset Timeout	Prog	Capacitor	Capacitor	Fixed
# of Voltage Monitors	1	0	1	1 or 2
Voltage Monitor Threshold	Prog	N/A	Fixed	Fixed/Resistor
Long Duration Manual Reset?	Prog	N	N	Fixed
Long Duration Input Range (s)	0.125-40	N/A	N/A	6.72
# External components	0	3	5	3
Package Type	CSP-6	DFN-8	SOT-23	SOT-23
Package Size (mm)	1.2x1.8	3x2	3x3	3x3
Price $ (1K est.)	$ 0.90	$ 1.75	$ 0.99	$ 1.25

World's smallest reset IC!



CSP packages and zero external components cut footprint 60%-90%!

Applications

- Handheld GPS Terminals
- Wireless LAN/WAN Cards
- 3G Phones
- PDA/Smartphones
- Digital Cameras/Camcorders
- Portable Media Players/Games

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productroundup

INTEGRATED CIRCUITS

Audio/video decoder integrates a 3-D-comb filter

Integrating the functions of multiple devices, the CX25845 audio/video decoder features a multiformat video decoder, a 3-D-comb filter, and a worldwide-broadcast audio decoder. The device also includes integrated SDRAM, enabling pin-for-pin compatibility with the previous generation's CX25480/1/2/3 product family. Available in a lead-free ETQFP (exposed-thin-quad-flat-pack)-80, the CX25845 costs $8.

Conexant Systems, www.conexant.com

Low-cost, floating-point DSP includes a preloaded ROM

Running at 200 MHz, the TMS320C6720 DSP includes 64 kbytes of on-chip RAM, a 32-kbyte instruction cache, and a 384-kbyte ROM. The ROM comes preloaded with DSP/BIOS, a real-time DSP kernel, and DSP libraries of commonly used functions. The device also features a dMax DMA engine. Pin-for-pin compatible with the TMS320C6722 and TMS320C6726 DSPs, the TMS320C6720 costs $5.75.

Texas Instruments, www.ti.com

Processor family doubles internal-bus bandwidth

Targeting automotive applications, the ADSP-BF54x family provides an increased I/O and memory bandwidth, on-chip memory, and integration of CAN (controller-area-network) and MOST (media-oriented-system-transport) peripherals. Joining the Blackfin series, the family embeds Lockbox Secure technology, protecting developers' software code. Additional features include increased internal-bus bandwidth to 532 Mbps and as much as 260 kbps of on-chip memory. Available in 400-, 533-, and 600-MHz operating speeds, the ADSP-BF542 costs $11.95 to $15.65. The ADSP-BF544 comes in 400- and 533-MHz options, and prices range from $13.25 to $15.35. The ADSP-BF548 comes in 533- and 600-MHz options, and prices range from $15.95 to $17.95. The ADSP-BF549 comes with 533-MHz speed and costs $18.58.

Analog Devices, www.analog.com

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LOOKING AHEAD

TO ANALOG VERSUS DIGITAL AT APEC 2007

The 22nd annual APEC (Applied Power Electronics Conference, www.apec-conf.org/) kicks off at the Disneyland Hotel in Anaheim, CA, on Feb 25. Billed as the must-attend conference for anyone involved in power electronics, APEC spans a range from the traditional and mature to the near-science-fiction in the power arena. Keynotes, for example, will include Texas Instruments fellow Bob Mammano on the history of power electronics, Fairchild Semiconductor President and Chief Executive Officer Mark Thompson on the future of power semiconductors, and, if that's not futuristic enough for you, Vatche Vorperian from CalTech's Jet Propulsion Laboratory on "Power Electronics at the Extremes of Possibility." Paper sessions will cover a similar range, this year giving center stage to a faceoff between digital and analog control of power circuits.

LOOKING BACK

AT DOCUMENT-QUALITY PRINTING

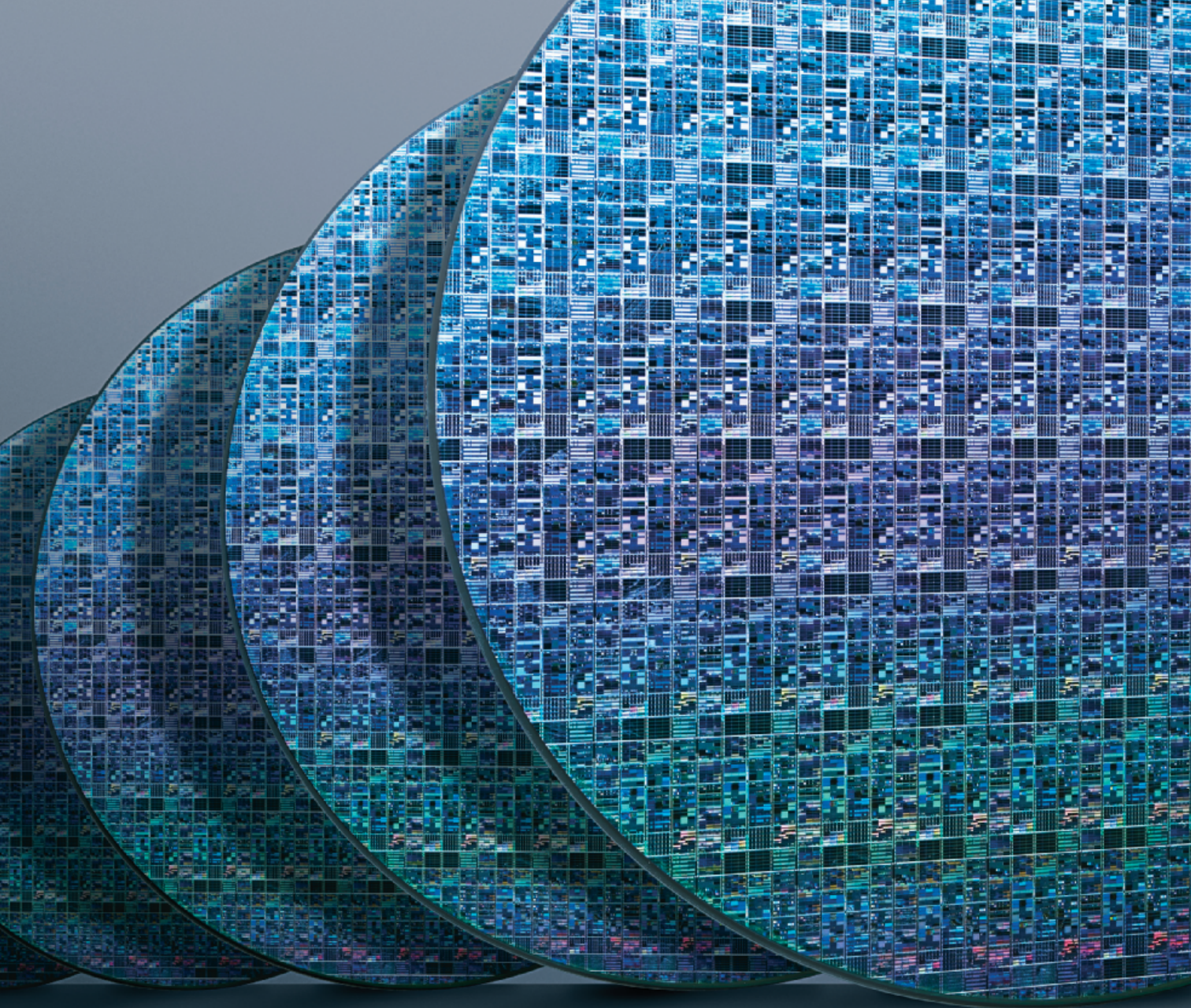
A solenoid-operated slave typewriter permits rapid recording of business and instrument data transmitted to it, providing written records at up to 11 characters per second. Produced by Underwood Corp, the slave machine is equipped with solenoids located in a compact control unit beneath the keyboard. Each solenoid depresses its associated key in response to impulses received through two miniature Cannon connector plugs for each solenoid. A feedback switch supplies a governing pulse back to the transmitting instrument to ensure proper coordination on character, space, backspace, carriage-return, and tab key actuation. Solenoid resistance is 1000Ω, and inductance is 0.77H at 100V dc and 100-mA drive.

—*Electrical Design News*, January 1957

LOOKING AROUND

AT THE GROWING INTEREST IN DEVELOPING-COUNTRY ELECTRONICS

Most of us still think of personal electronics as an industrialized-world phenomenon: a market that requires an affluent middle class. But, as the affluent markets for high-end electronic gear begin to saturate—as they are apparently beginning to do—more and more attention is turning to electronics for the still-developing world. The emergence of microfinance and the runaway success of, for example, cellular-service providers in Africa, have demonstrated that people with little income can still obtain and benefit from cell phones, computers, Internet connections, and media players. More important for vendors, they can make money providing these things. So, 2007 will be a year of low-end platforms, particularly in cellular handsets and Internet-capable PCs. These devices may provide some of the most interesting design challenges of the decade.



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